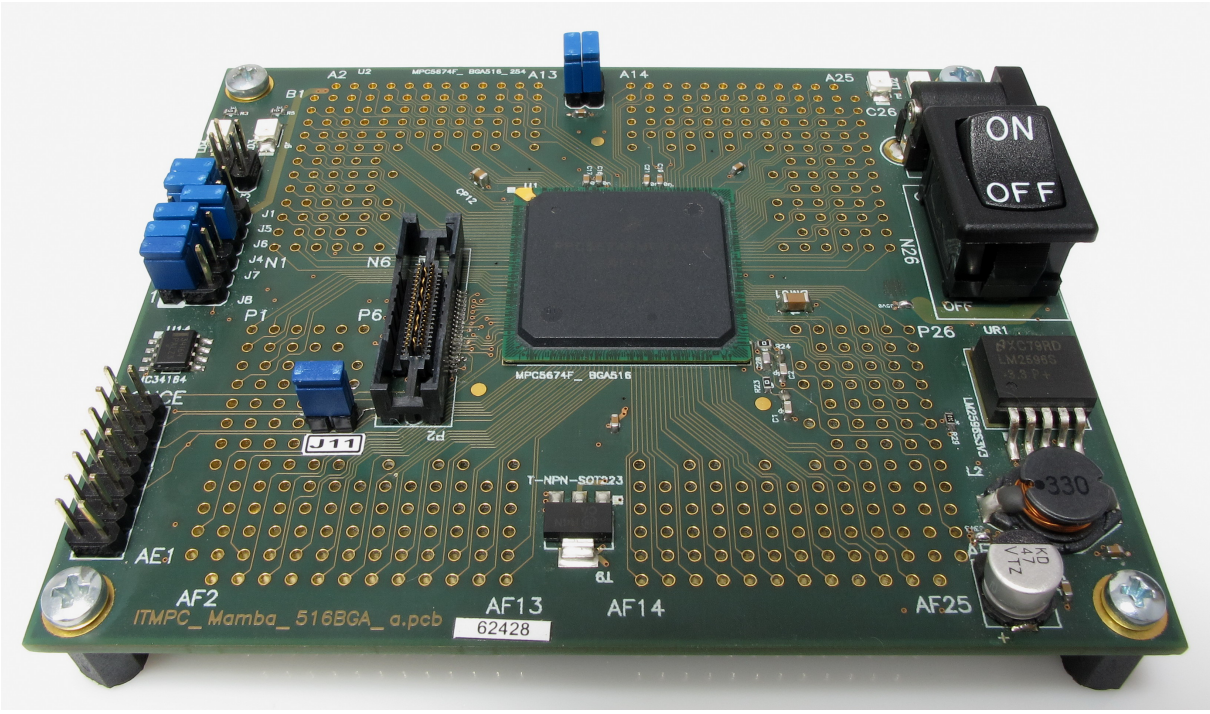
User's Manual

Freescale MPC5674F Target Board

	Ordering code
MPC5674F Target Board	**ITMPC5674F_516**



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Contents

Features

This target board is an evaluation and a development system for the Freescale MPC5674F microcontroller. The ITMPC5674F package consists of a power supply and a target board populated with the Freescale MPC5674F CPU in the BGA516 package, JTAG debug and Nexus debug connectors. The application under the development or test can run from the internal CPU flash or from the internal SRAM.

Specifications

Clock Speed – up to 132 MHz
Power requirement: 6 - 12V DC , + in the center @ 500 mA
Power output: 5V, 3.3V, and 2.5V regulated supplies
Board Size: 106 mm x 86 mm

EVB-5674F Features

- MPC5674F, BGA516
- 8MHz clock (ext. crystal)
- Power Indicators – Supply voltage indications for 3.3V
- User Indicator – two user indicators to provide user conceived visual response during testing
- Configuration jumper - Jumpers J1, J4 to J10 configures processor startup mode; Jumper J11 selects debugging via ONCE.
- Two debug options available – JTAG (ONCE), Nexus

Software Development

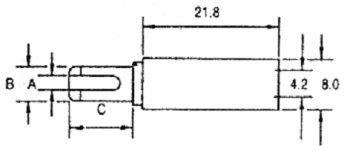
The board has been tested and does run at speeds up to 132 MHz, which you can set by engaging the PLL module in your software. Software development on the board can be performed using the iSYSTEM IC3000 or IC5000 tools, which can be connected to the ONCE (JTAG) or P2 (Nexus) connector. This provides real-time access to all hardware, peripherals and memory on the board.

Getting Started - Setting up the EVB-5674F Board

Power Supply

Permissible input voltage: 6-12 V DC, **+ in the center.** The required current load capacity of the power supply depends on the specific configuration of the target board. A power supply with a minimum of 500mA is recommended and delivered in the package. Low voltage DC plug must conform to the DIN 45323 standards:

- The hole diameter is 1.95 – 2.5 mm (standard: 2.1 mm)
- The external diameter is 6.2 - 5.5 mm (standard: 5.5 mm)



Dimensions

A	B	C
2.1	5.5	9.5

Switch-on the target board after the AC power supply is plugged into the wall and connected to the target board. Check that power indicator (LD1) lit, indicating that 3.3V voltage is present.

Note: When connecting an external debugger, make sure that the emulator is powered on first, then the target board and vice versa when switching off the system. First, switch off the target and then the emulator.

Troubleshooting

EVB-5674F doesn't show signs of life by first start

a) Check the power supplied to the EVB board – Diode LD1.

b) When connecting the JTAG debugger via ONCE connector, make sure that Jumper J11 is set. When Jumper J11 is not set, a connection via Nexus port must be made.

c) Try "slow" JTAG Scan Speed if the debugger cannot connect to the CPU.

d) Execute debug Reset instead of the debug Download.

Unable to download the code to the board

a) Check the power supplied to the EVB board.

b) Ensure that the correct workspace was loaded into winIDEA.

c) Check the hardware configuration:

- Hardware>Hardware …
- Hardware>Emulation Options

d) Reset the board and try to connect again.

Checksum failed error

a) When performing any kind of checksum, remove all software breakpoints

Settings and Options

Jumpers

Jumpers J1, J4 to J10 configures processor startup mode. See MPC5674F Reference Manual for more details on the CPU signals BOOTCFG[0:1], PLLCFG[0:2], WKPCFG, VRH and VRL.

Jumper J11 selects whether debugger works via JTAG (ONCE) or via Nexus port.

Jumper J2 connects user LD4 LED to the CPU pin GPIO89 and jumper J3 connects user LD3 LED to the CPU pin GPIO90.

Jumper pin 1 is marked with a white square on the ITMPC5674F PCB. If pin 1 cannot be located directly from the ITMPC5674F, please use Figure 2 for assistance.

Note: Don't change jumper settings while the ITMPC5674F Target Board is supplied with the power!

J1	**BOOTCFG0**
1-2*	BOOTCFG0 = 0
2-3	BOOTCFG0 = 1
J5	**BOOTCFG1**
1-2*	BOOTCFG1 = 0
2-3	BOOTCFG1 = 1
J6	**PLLCFG0**
1-2	PLLCFG0 = 0
2-3*	PLLCFG0 = 1
J4	**PLLCFG1**
1-2*	PLLCFG1 = 0
2-3	PLLCFG1 = 1

J7	**PLLCFG2**
1-2*	PLLCFG1 = 0
2-3	PLLCFG1 = 1
J8	**WKPCFG**
1-2*	WKPCFG = 0
2-3	WKPCFG = 1
J9	**VRH**
Closed*	VRH set to 5V
Open	VRH not connected
J10	**VRL**
Closed*	VRL set to GND
Open	VRL not connected
J11	**Debug mode**
Closed*	Debugging via JTAG port
Open	Debugging via Nexus port

Figure 1: Jumper configuration (* - default position)

Status Indicators

One LED diode show the presence of supply voltage +3.3V. LD01 (+3.3V) must light when the power is applied to the evaluation board.

LD3 and LD4 are available for the user.

LD2 shows reset line status.

Component List

Name	Description
U1	Motorola MPC5674F CPU
P2	Nexus debug connector
P1	Power supply connector
ONCE	JTAG debug connector
J2	Connects LD4 to CPU GPIO89
J3	Connects LD3 to CPU GPIO90
J1	BOOTCFG0
J5	BOOTCFG1
J6	PLLCFG0
J4	PLLCFG1
J7	PLLCFG2
J8	WKPCFG
J9	VRH
J10	VRL
J11	Debug connector selection
LD1	Power LED 3,3V
LD2	Reset indication LED
LD3	User LED
LD4	User LED
SW1	Power switch

Connectors

14-pin JTAG debug connector (ONCE)

CPU_TDI	**1**	**2**	GND
CPU_TDO	**3**	**4**	GND
CPU_TCK	**5**	**6**	GND
N.C.	**7**	**8**	N.C.
CPU_RESET	**9**	**10**	CPU_TMS
3V3	**11**	**12**	N.C.
N.C.	**13**	**14**	CPU_TRST

External JTAG debug tool connects to a 14-pin JTAG debug connector. **Jumper J11 must be closed when using debugger via JTAG (ONCE) port.**

Nexus 38-pin Mictor debug connector

Signal	Pin	Pin	Signal
MDO12	1	2	MDO13
MDO14	3	4	MDO15
MDO9	5	6	Not used
Not used	7	8	MDO8
RSTIN	9	10	EVTIN
TDO	11	12	VTREF
MDO10	13	14	RDY
TCK	15	16	MDO7
TMS	17	18	MDO6
TDI	19	20	MDO5
NTRST	21	22	MDO4
MDO11	23	24	MDO3
Not used	25	26	MDO2
Not used	27	28	MDO1
Not used	29	30	MDO0
Not used	31	32	EVTO
Not used	33	34	MCKO
Not used	35	36	MSEO1
Not used	37	38	MSEO0

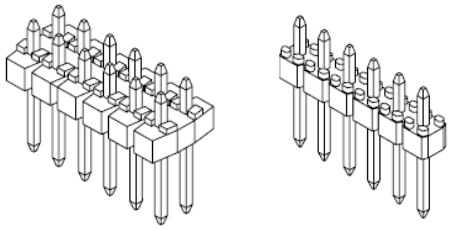
External Nexus debug tool connects to a Nexus 38-pin Mictor debug connector. **Jumper J11 must be open when using debugger via Nexus port.**

CPU expansion connector

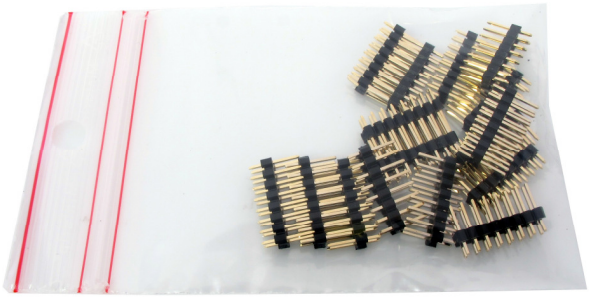
The CPU expansion connector makes all the CPU signals accessible and can be used in order to expand the development system by connecting the ITMPC5674F to another module. The CPU expansion connector uses the same numbering scheme as the original CPU in the BGA516 package. The CPU expansion connector builds the matrix that matches with the CPU BGA516 pinout.

By populating the expansion array with 2.54mm pitch headers, the board can be easily connected to another custom tailored board.

An example of breakaway dual and single row 2.54mm pitch headers, which can be easily stacked side-to-side:

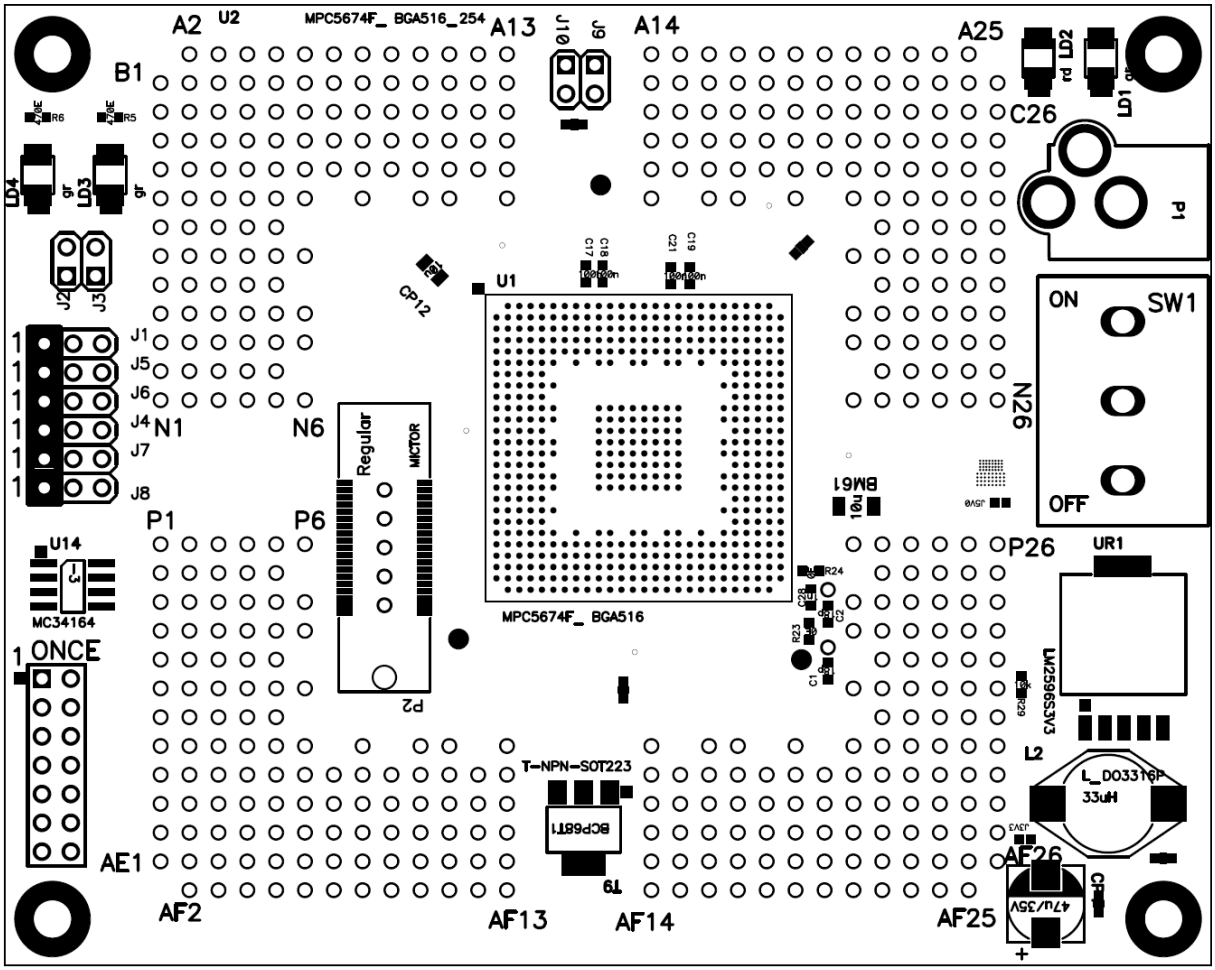


A small plastic bag with headers comes along the target board already.



Appendix A

View of the ITMPC5674F

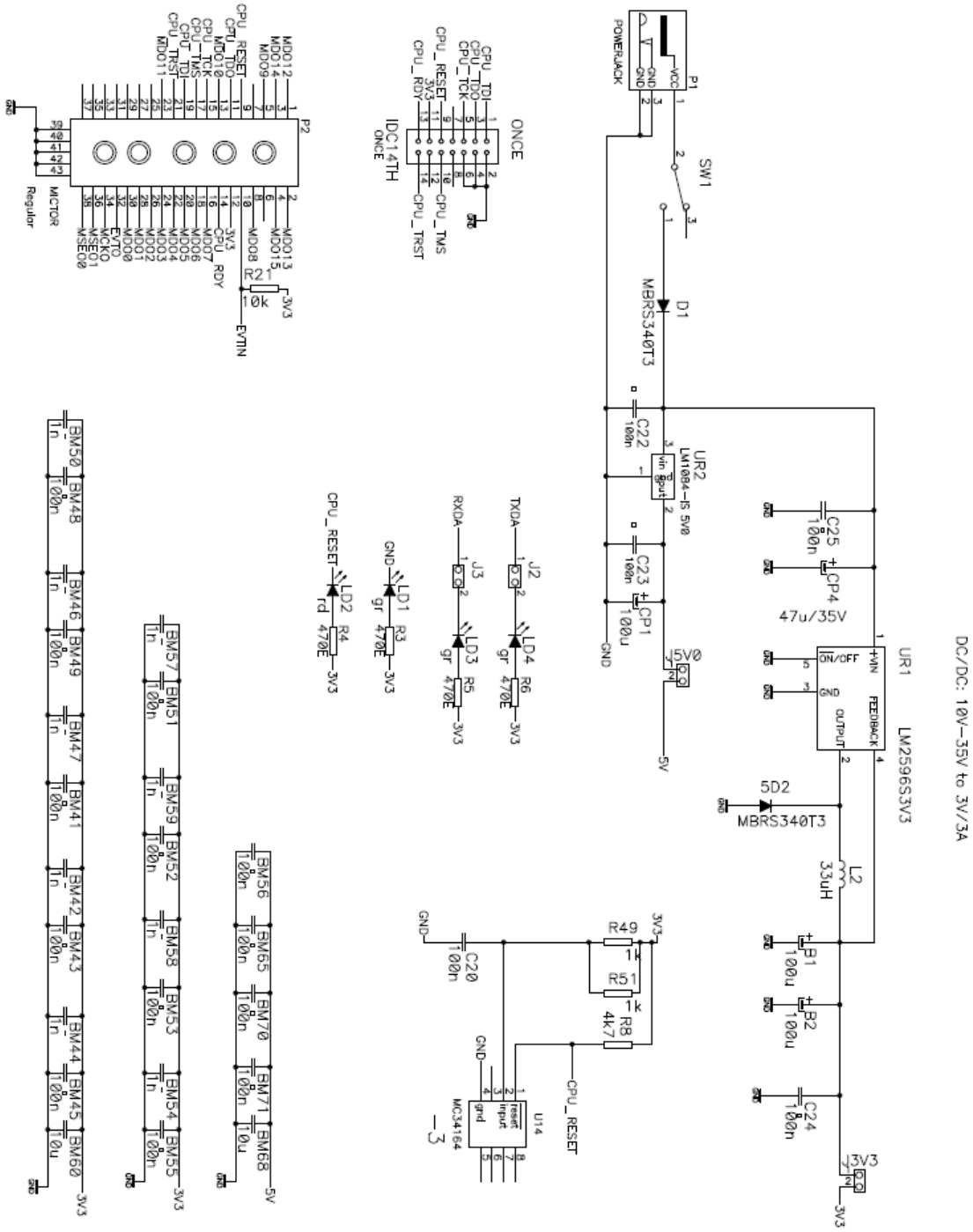


Note: A designation on *Figure 4* stands for A1 designation on the above ITMPC5674F view, B stands for B1, AF stands for AF1 etc.

Expansion Connector as seen from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDD	RSTOUT	ANA0	ANA4	ANA9	ANA11	ANA15	VDDA_A0	REF-BYPCA1	VRL_A	VRH_A	AN28	AN29	AN36	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	VDDEH1	VSS	VDD	TEST	ANA1	ANA5	ANA10	ANA14	VDDA_A1	VSSA_A1	REF-BYPCA	AN24	AN27	AN30	AN32	VDDA_B1	VSSA_B0	REF-BYPCB	ANB4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2	ANA6	ANA7	ANA13	ANA17	ANA19	ANA21	ANA22	AN25	AN31	AN34	AN39	AN37	ANB0	ANB7	ANB6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3	ANA8	ANA12	ANA16	ANA18	ANA20	ANA23	AN26	AN33	AN35	AN38	ANB1	ANB2	ANB3	ANB14	ANB16	ANB17	VSS	VDDEH7	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18																	ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16															ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12																	ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10															ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	PLLCFG1	PLLCFG2	BOOT-CFG1	BOOT-CFG0	RXDB	ETPUA0															VDD33_6	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	VDD33_1	D_BDIP	PLLCFG0	VSTBY	WKPCFG																	D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8															VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	VDD33_1															VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16																	ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3															ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0															ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V	EVTI	EVTO	MDO0	MDO2	MDO3																	ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1															ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y	MDO7	MDO9	MDO10	MDO11	MDO12																	ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	MDO13	MDO14	MDO15	VDD33_1	VDDE8	VSS		PCSA5		SOUTB	VDD33_4		VDDE9	VDD33_4		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDD33_3	ETPUB28	VDDREG	VSSSYN	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSFL	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF		VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Schematic


DC/DC: 10V-35V to 3V/3A
UR1
LM2596S3V3
+VIN
FEEDBACK
ON/OFF
GND
OUTPUT
47u/35V
5D2
MBRS340T3
L2
33uH
P1
100u
P2
100u
C24
100n
J3V3
3V3
C25
100n
CP4
UR2
LM1084-IS 5V0
vin
gout
C22
100n
C23
100n
CP1
100u
5V0
5V
D1
MBRS340T3
SW1
P1
POWERJACK
VCC
GND
ONCE
IDC14TH
CPU_TDI
CPU_TDO
CPU_TCK
CPU_RESET
3V3
CPU_RDY
CPU_TMS
CPU_TRST
P2
MICTOR
Regulator
MD012
MD014
MD009
MD013
MD015
MD008
3V3
CPU_RDY
MD007
MD006
MD005
MD004
MD003
MD002
MD001
MD000
EVTO
MCKO
MSEO1
MSEO0
R21
10k
EVTIN
J2
TXDA
LD4
gr
R6
470E
3V3
J3
RXDA
LD3
gr
R5
470E
3V3
LD1
gr
R3
470E
3V3
LD2
rd
R4
470E
3V3
CPU_RESET
U14
MC34164
reset
input
gnd
C20
100n
R49
1k
R51
1k
R8
4k7
3V3
CPU_RESET
BM50
BM48
BM46
BM49
BM47
BM41
BM42
BM43
BM44
BM45
BM60
BM57
BM51
BM59
BM52
BM58
BM53
BM54
BM55
BM56
BM65
BM70
BM71
BM68
1n
100n
10u
3V3
5V