

---

## POD Hardware Reference

### AM186EM POD rev. D

Ordering code	IC20015
---------------	---------



Thank you for purchasing this product from iSYSTEM. This product has been carefully crafted to satisfy your needs. Should any questions arise, do not hesitate to contact your local distributor or iSYSTEM directly. Our technical support personnel will be happy to answer all your technical support questions.

All information, including contact information, is available on our web site [www.isystem.com](http://www.isystem.com). Feel free also to explore our alternative products.

iSystem constantly yields for development and therefore certain pictures in this documentation may vary slightly from the actual product you received. The differences should be minor, but should you find more serious inconsistencies of the product with the documentation, please contact your local distributor for more information.

This document and all documents accompanying it are copyrighted by iSYSTEM and all rights are reserved. Duplication of these documents is allowed for personal use. For every other case a written consent from iSYSTEM is required.

Copyright © 2006 iSYSTEM, GmbH.  
All rights reserved.  
All trademarks are property of their respective owners.

## POD Hardware Reference

### In-Circuit Emulation PODs

The following elements of interest are located on all In-Circuit emulation PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED (D3) - lit when CPU is running
- green LED (D4) - lit when Emulator is ready for emulation
- a connector, mostly marked ST3 - contains signal lines, some of which are hardware configuration lines (such as bank select signals), others you can use for signal generation (pattern generator outputs).

Here are some common signals found on the signal connector, commonly marked as ST3:

- GND            Ground
- BPE            External breakpoint input. Active high.
- RESO/RO      Reset output. Connect to target to reset peripherals.
- TRES/TR      Target reset input.
- AUXn          AUX signal inputs (same as inputs on Emulator/trace)

---

Note: On PODs that support synchronization between two or more Emulators (currently only the HC(S)12 Family, see the Synchronization section in the Hardware User's Guide for more information) AUX0 and AUX1 are cut short with Run/Stop synchronization line, and AUX2, AUX3 with RESET synchronization line. You should use these pins to connect to other PODs or target CPUs.

---

- PAT0-2        Pattern generator output on 16-bit POD
- OC4-6        Pattern generator output on 8-bit POD

---

Note: The signal connector can also have other markings, like P1, U1, etc. Please refer to the POD-specific documentation for the signal connector name and signals present.

---

For every POD the following information is given:

- Ordering code. If there are different speed versions of a POD the ordering code is modified by appending the speed in MHz (IC81020-16 for the 16 MHz 8031 POD)
- information on available speed versions and required Emulator access time
- POD size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

---

Note: The In-Circuit Emulator can emulate a processor or a microcontroller. Beside the CPU, additional logic is integrated on the POD. The amount of additional logic depends on the emulated CPU and the type of emulation. A buffer on a data bus is always used (minimal logic) and when rebuilding ports on the POD, maximum logic is used. As soon as a POD is inserted in the target instead of the CPU, electrical and timing characteristics are changed. Different electrical and timing characteristics of used elements on the POD and prolonged lines from the target to the CPU on the POD contribute to different POD characteristics. Consequently, signal cross-talks and reflections occur, capacitance changes, etc.

Beside that, pull-up and pull-down resistors are added to some signals. Pull-up/pull-down resistors are required to define the inactive state of signals like reset and interrupt inputs, while the POD is not connected to the target. Because of this, the POD can operate as standalone without the target.

---

## Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

## For Better Understanding of the Hardware Reference: PIN 1 locations

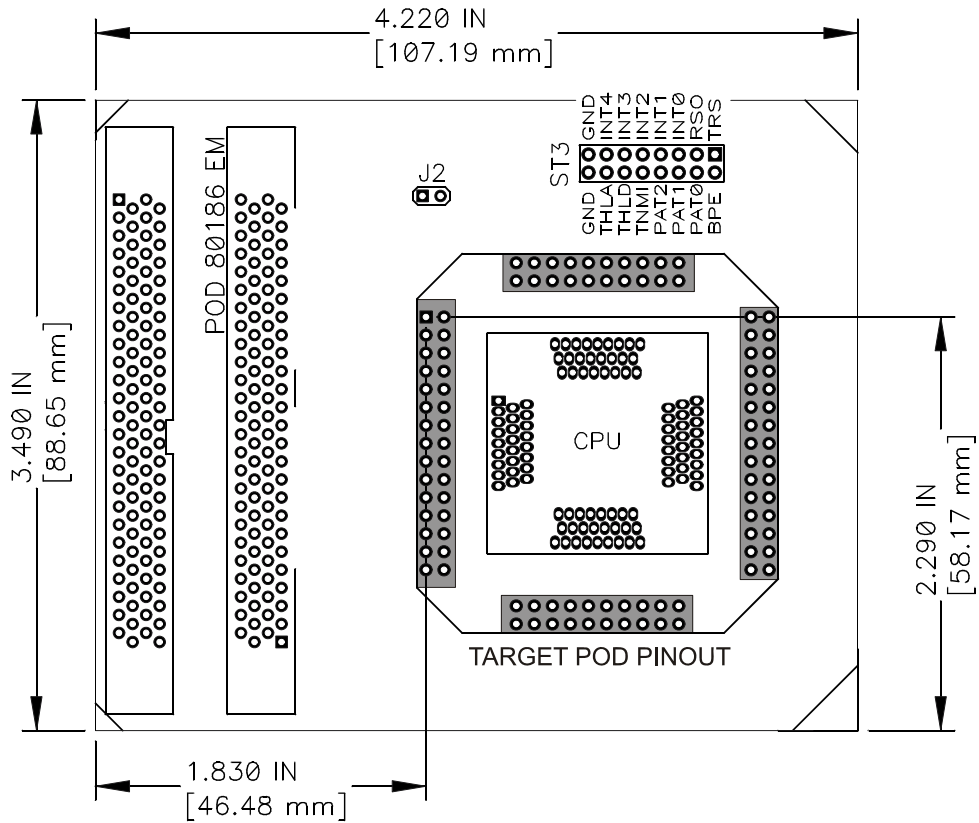
There are several references to pin 1 in the manual and many jumper settings, CPU and pinout orientations rely on the correct location of pin 1. If sometimes the location of pin 1 is not clear, check the markings on the POD. If there are no markings, check the PCB board of the POD. Pin 1 is always marked on the PCB with a square pin (the other pins are round). The pin 1 location is also visible on the board in the hardware reference, if not any other way it can be identified by searching for the square pin.

# POD Hardware Reference

## AM186EM POD rev. D

<b>Ordering code</b>	<b>IC20015</b>	
<b>POD Speed (MHz)</b>	<b>20</b>	<b>40</b>
<b>Emulator Speed (ns)</b>	<b>90</b>	<b>65</b>
<b>Exchange CPU</b>	<b>YES</b>	
<b>Dimensions (mm)</b>	<b>107x88</b>	
<b>Pin 1 position (mm)</b>	<b>47x57</b>	

Please make sure you have read the technical notes on the Intel 80x86 Family in the Hardware User's Guide before connecting the POD.



POD View

Emulated CPUs
Am186 EM(LV)
Am186 ES(LV)
Am188 EM(LV)
Am188 ES(LV)
Am186 ER
Am188 ER

Do note that there are two PODs available for these types of CPU: the IC20014 and the IC20015. The only difference is the size of the CPU, which can be inserted into the POD.

POD	CPU Size
<b>IC20014</b>	14 x 14 mm
<b>IC20015</b>	14 x 20 mm

*POD Selection guide*

## Voltage Settings

This POD supports both 5V and 3.3 V CPUs. The operation voltage is defined by the J2 jumper.

V <sub>CC</sub> level	J2 setting
3.3 V	Removed
5.0 V	Set (*)

*Jumper J2 settings (\* - factory default)*

## Emulation Notes

### *80186 ES Operation*

On 80186 ES, the UCS and LCS must always be initialized with 16-bit access (in UCS address range).

### *Pin Configuration*

The following pins must be configured in this way in order for the Emulator to operate in normal mode:

- A17 = IO7
- A18 = IO8
- A19 = IO9
- S6 = IO29
- CLKOUTA

## The Signal Connectors

A signal connector is present on this pod, marked as ST3.

Description	Signal	Pin	Pin	Signal	Description
Target Reset Input	TRS	1	2	BPE	External Breakpoint Input
Reset Output	RSO	3	4	PAT0	Pattern Generator Output
Interrupt Input Line	INT0	5	6	PAT1	Pattern Generator Output
Interrupt Input Line	INT1	7	8	PAT2	Pattern Generator Output
Interrupt Input Line	INT2	9	10	TNMI	NMI Input Line
Interrupt Input Line	INT3	11	12	THLD	HOLD Line Input
Interrupt Input Line	INT4	13	14	THLA	HLDA Line Output
Ground	GND	15	16	GND	Ground

### *ST3 Connector signals*

The Interrupt Input lines can be used to assert interrupts to CPU when operating without target.

The NMI input line can be used to assert the NMI interrupt to CPU when operating without a target.

# POD Target Layout

The POD target layout is T\_QFP100.

79	77	75	73	71	69	67	65	63	61	59	57	55	53	51
80	78	76	74	72	70	68	66	64	62	60	58	56	54	52

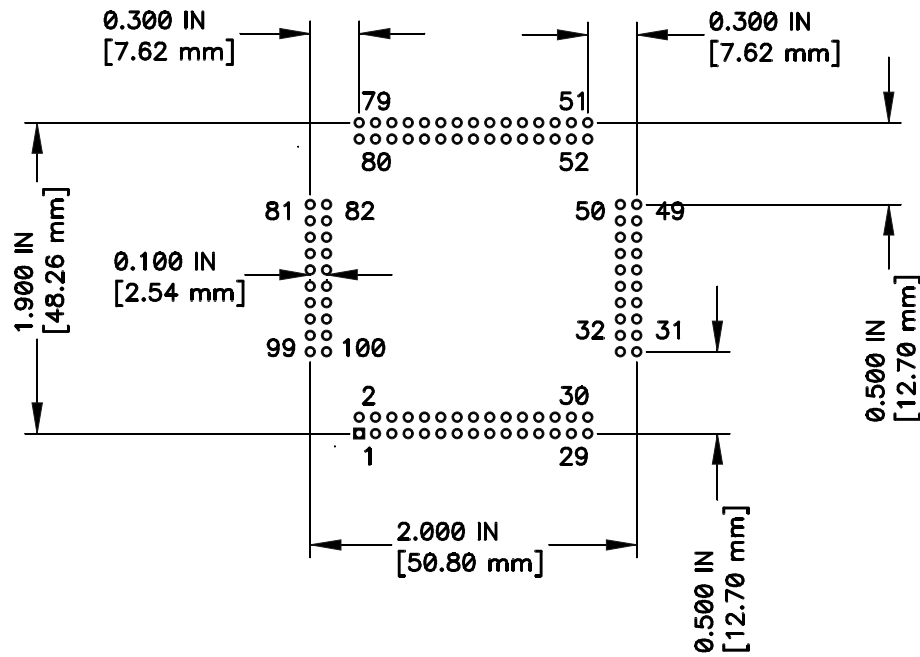
81	82
83	84
85	86
87	88
89	90
91	92
93	94
95	96
97	98
99	100

50	49
48	47
46	45
44	43
42	41
40	39
38	37
36	35
34	33
32	31

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29

*T\_QFP100 Target POD Layout, Top view*

Please put special attention to the PIN1 position as marked on the POD to get the correct view of the POD layout.



*T\_QFP100 Pinout Dimensions*

Notes: