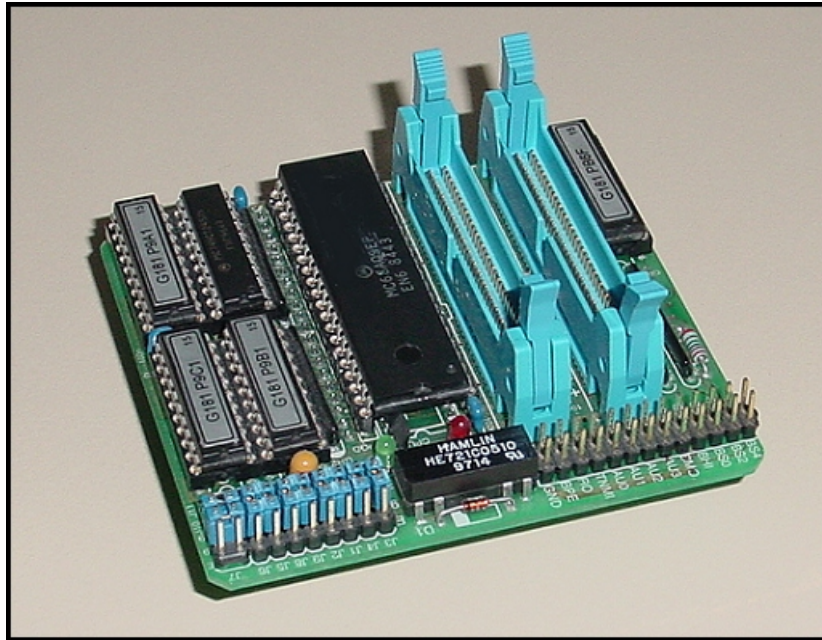

POD Hardware Reference

Motorola 6809 B POD rev. C

Ordering code	IC81060
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POD Hardware Reference

In-Circuit Emulation PODs

The following elements of interest are located on all In-Circuit emulation PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED (D3) - lit when CPU is running
- green LED (D4) - lit when Emulator is ready for emulation
- a connector, mostly marked ST3 - contains signal lines, some of which are hardware configuration lines (such as bank select signals), others you can use for signal generation (pattern generator outputs).

Here are some common signals found on the signal connector, commonly marked as ST3:

- GND Ground
- BPE External breakpoint input. Active high.
- RESO/RO Reset output. Connect to target to reset peripherals.
- TRES/TR Target reset input.
- AUXn AUX signal inputs (same as inputs on Emulator/trace)

Note: On PODs that support synchronization between two or more Emulators (currently only the HC(S)12 Family, see the Synchronization section in the Hardware User's Guide for more information) AUX0 and AUX1 are cut short with Run/Stop synchronization line, and AUX2, AUX3 with RESET synchronization line. You should use these pins to connect to other PODs or target CPUs.

- PAT0-2 Pattern generator output on 16-bit POD
- OC4-6 Pattern generator output on 8-bit POD

Note: The signal connector can also have other markings, like P1, U1, etc. Please refer to the POD-specific documentation for the signal connector name and signals present.

For every POD the following information is given:

- Ordering code. If there are different speed versions of a POD the ordering code is modified by appending the speed in MHz (IC81020-16 for the 16 MHz 8031 POD)
- information on available speed versions and required Emulator access time
- POD size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

Note: The In-Circuit Emulator can emulate a processor or a microcontroller. Beside the CPU, additional logic is integrated on the POD. The amount of additional logic depends on the emulated CPU and the type of emulation. A buffer on a data bus is always used (minimal logic) and when rebuilding ports on the POD, maximum logic is used. As soon as a POD is inserted in the target instead of the CPU, electrical and timing characteristics are changed. Different electrical and timing characteristics of used elements on the POD and prolonged lines from the target to the CPU on the POD contribute to different POD characteristics. Consequently, signal cross-talks and reflections occur, capacitance changes, etc.

Beside that, pull-up and pull-down resistors are added to some signals. Pull-up/pull-down resistors are required to define the inactive state of signals like reset and interrupt inputs, while the POD is not connected to the target. Because of this, the POD can operate as standalone without the target.

Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

For Better Understanding of the Hardware Reference: PIN 1 locations

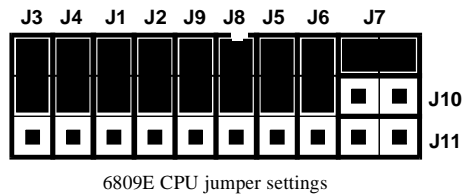
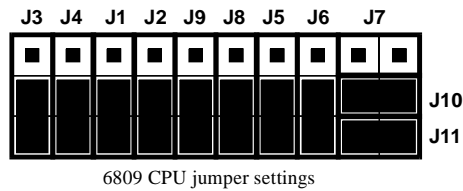
There are several references to pin 1 in the manual and many jumper settings, CPU and pinout orientations rely on the correct location of pin 1. If sometimes the location of pin 1 is not clear, check the markings on the POD. If there are no markings, check the PCB board of the POD. Pin 1 is always marked on the PCB with a square pin (the other pins are round). The pin 1 location is also visible on the board in the hardware reference, if not any other way it can be identified by searching for the square pin.

Inserted CPU Information

Normally, a 68A09E CPU is inserted in the POD. For emulation, the proper speed version of the CPU must be inserted and the CPU must always be of type 6809E (i.e. 6809E, 68A09E, 68B09E). The CPU selection jumpers must be configured according to the emulated CPU type – whether the emulated CPU is of type 6809 or 6809E.

CPU Selection

There are 11 jumpers on the POD that define which CPU is being emulated.



Note:

- when 6809 CPU is emulated the clock can be retrieved either from the Emulator internal clock or from the target system oscillator. When the target system is using quartz, then only the Emulator internal clock can be used.
- when the 6809E is used with a target system, the Emulator's internal clock can not be used, because other target devices probably use the external E and Q also. (Target and CPU must use the same clock).

The Signal Connector

A signal connector is present on the POD, named ST3.

Description	Signal	Pin	Pin	Signal	Description
Ground	GND	1	2	GND	Ground
External Breakpoint	BPE	3	4	FI	Target FI
Reset Output	RO	5	6	IRQ	Target IRQ
Target NMI	TNMI	7	8	TR	Target Reset
Auxilliary Input	AUX0	9	10	n.c.	Not used
Auxilliary Input	AUX1	11	12	OC4	Pattern Generator Output
Auxilliary Input	AUX2	13	14	OC5	Pattern Generator Output
Auxilliary Input	AUX3	15	16	OC6	Pattern Generator Output
Bridge this pin always to GND	BMO	17	18	GND	Ground
Not used	n.c.	19	20	GND	Ground
Bank select line for memory banking	BS0	21	22	BS1	Bank select line for memory banking
Bank select line for memory banking	BS2	23	24	BS3	Bank select line for memory banking
Bank select line for memory banking	BS4	25	26	n.c.	Not used

ST3 signal connector pinout

Target POD Pinout

This PODs support the standard DIP40 pinout.

Notes:

Notes: