
POD Hardware Reference

In-Circuit Emulation PODs

The following elements of interest are located on all In-Circuit emulation PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED (D3) - lit when CPU is running
- green LED (D4) - lit when Emulator is ready for emulation
- a connector, mostly marked ST3 - contains signal lines, some of which are hardware configuration lines (such as bank select signals), others you can use for signal generation (pattern generator outputs).

Here are some common signals found on the signal connector, commonly marked as ST3:

- GND Ground
- BPE External breakpoint input. Active high.
- RESO/RO Reset output. Connect to target to reset peripherals.
- TRES/TR Target reset input.
- AUXn AUX signal inputs (same as inputs on Emulator/trace)

Note: On PODs that support synchronization between two or more Emulators (currently only the HC(S)12 Family, see the Synchronization section in the Hardware User's Guide for more information) AUX0 and AUX1 are cut short with Run/Stop synchronization line, and AUX2, AUX3 with RESET synchronization line. You should use these pins to connect to other PODs or target CPUs.

- PAT0-2 Pattern generator output on 16-bit POD
- OC4-6 Pattern generator output on 8-bit POD

Note: The signal connector can also have other markings, like P1, U1, etc. Please refer to the POD-specific documentation for the signal connector name and signals present.

For every POD the following information is given:

- Ordering code. If there are different speed versions of a POD the ordering code is modified by appending the speed in MHz (IC81020-16 for the 16 MHz 8031 POD)
- information on available speed versions and required Emulator access time
- POD size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

Note: The In-Circuit Emulator can emulate a processor or a microcontroller. Beside the CPU, additional logic is integrated on the POD. The amount of additional logic depends on the emulated CPU and the type of emulation. A buffer on a data bus is always used (minimal logic) and when rebuilding ports on the POD, maximum logic is used. As soon as a POD is inserted in the target instead of the CPU, electrical and timing characteristics are changed. Different electrical and timing characteristics of used elements on the POD and prolonged lines from the target to the CPU on the POD contribute to different POD characteristics. Consequently, signal cross-talks and reflections occur, capacitance changes, etc.

Beside that, pull-up and pull-down resistors are added to some signals. Pull-up/pull-down resistors are required to define the inactive state of signals like reset and interrupt inputs, while the POD is not connected to the target. Because of this, the POD can operate as standalone without the target.

Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

For Better Understanding of the Hardware Reference: PIN 1 locations

There are several references to pin 1 in the manual and many jumper settings, CPU and pinout orientations rely on the correct location of pin 1. If sometimes the location of pin 1 is not clear, check the markings on the POD. If there are no markings, check the PCB board of the POD. Pin 1 is always marked on the PCB with a square pin (the other pins are round). The pin 1 location is also visible on the board in the hardware reference, if not any other way it can be identified by searching for the square pin.

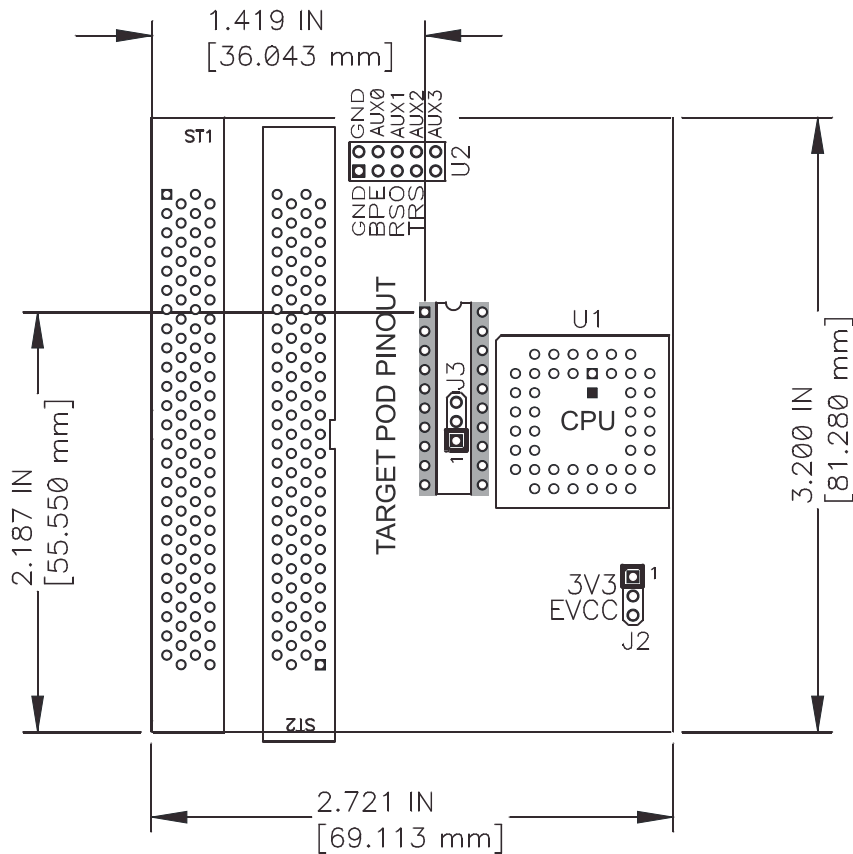
POD Hardware Reference

Philips P87LPC769 POD rev. A

Ordering code	IC10023
POD Speed (MHz)	20
Emulator Speed (ns)	65
Bank switch support	NO
Exchange CPU	NO

This POD can be used on iC1000 and the PowerEmulator unit. This POD can not be used with iC181.

Before connecting the PODs, make sure you have read the technical notes on Intel 8051 Family in the Hardware User's Guide.



The POD board

Emulated CPUs
Philips P87LPC760
Philips P87LPC761
Philips P87LPC762
Philips P87LPC764
Philips P87LPC767
Philips P87LPC769

Voltage Settings

If the POD is powered from the Emulator, the jumper J2 selects the V_{CC} level.

V_{CC} level	J2 setting
3.3 V	1-2
5.0 V	2-3

Jumper J2 settings

Additional Configuration

The LPC microcontrollers contain the register UCFG1 (User Configuration Register 1) with which various options are set. The register is available to the CPU on the XDATA address 0xFD00. With this pin the watchdog, external reset pin, etc. can be defined.

The UCFG1 register can not be programmed, since a bondout chip is used; instead, its value is set in the 'CPU Setup/Advanced' dialog.

A special function of the LPC family is the configuration of the CPU clock circuit. The clock circuit is also defined in the UCFG1 register. The default value is that the internal RC oscillator is selected, so that the POD is operational also without the target.

The jumper J3 defines the CPU pin P2.1 connection, the alternate function of which is the X1 clock input. The pin can be connected to the target or the emulator clock.

Pin P2.1 connection	J3 setting
Target	1-2
Emulator clock	2-3

Jumper J3 settings

POD Limitations

Between the addresses 0xFCE0 and 0xFCFF a so-called 32-byte customer code space is available. This area is not ment for program data, because it contains different data like software version, checksum, serial number or similar. This area can only be accessed with an MOVC instruction.

When a POD is used, a limitation is implied by the bondout chip: when this area is read, the CPU reads the internal memory and discards the 'external' information. This means that the download of this area can not be performed, since the CPU does not read it. If the 32-byte customer code space should be read, this area should be remapped to the area below 0x8000.

Setting CPU options

The **Operating Mode** (see Advanced In-Circuit Emulation Options on the 8051 Family in the Hardware User's guide) must be selected. The POD will always operate in the mode selected in software – the target EA is ignored.

If the **External XDATA enabled** option (see Advanced In-Circuit Emulation Options on the 8051 Family in the Hardware User's guide) is set, the CPU will generate an external cycle (P0, P2, RD and WR) every time a MOVX instruction is executed.

In a single chip application where only the internal XDATA memory is used and P0 and P2 are used by the application, this option must be disabled.

The **Stop CPU Activities when Stopped** option (see CPU Options in the Hardware User's guide) is functional only in **Single Chip** mode.

The Signal Connector

A signal connector is present on the POD, named U2:

Description	Signal	Pin	Pin	Signal	Description
Ground	GND	1	2	GND	Ground
External Breakpoint	BPE	3	4	AUX0	Auxilliary Input
Reset Output	RSO	5	6	AUX1	Auxilliary Input
Target Reset Input	TRS	7	8	AUX2	Auxilliary Input
Reserved	RSVD	9	10	AUX3	Auxilliary Input

U2 signal connector pinout and description

Target Adapters

iSYSTEM offers various adapter solutions for this POD. Please refer to the adapter documentation for more details.

POD Target Layout

Target POD pinout is standard DIP20.

Adapters for standard DIP14 and DIP16 pinouts are also available.

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