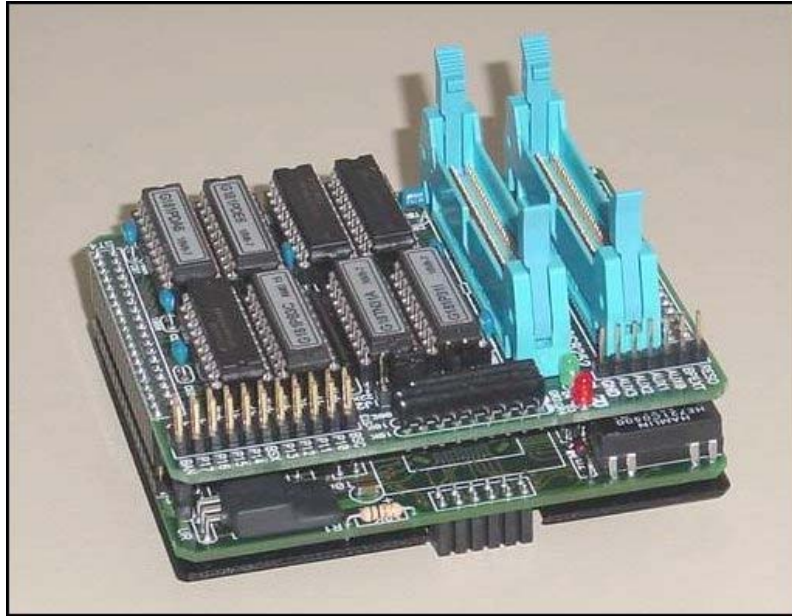

POD Hardware Reference

Intel 8031 POD rev. G

Ordering code	IC81020
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POD Hardware Reference

In-Circuit Emulation PODs

The following elements of interest are located on all In-Circuit emulation PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED (D3) - lit when CPU is running
- green LED (D4) - lit when Emulator is ready for emulation
- a connector, mostly marked ST3 - contains signal lines, some of which are hardware configuration lines (such as bank select signals), others you can use for signal generation (pattern generator outputs).

Here are some common signals found on the signal connector, commonly marked as ST3:

- GND Ground
- BPE External breakpoint input. Active high.
- RESO/RO Reset output. Connect to target to reset peripherals.
- TRES/TR Target reset input.
- AUXn AUX signal inputs (same as inputs on Emulator/trace)

Note: On PODs that support synchronization between two or more Emulators (currently only the HC(S)12 Family, see the Synchronization section in the Hardware User's Guide for more information) AUX0 and AUX1 are cut short with Run/Stop synchronization line, and AUX2, AUX3 with RESET synchronization line. You should use these pins to connect to other PODs or target CPUs.

- PAT0-2 Pattern generator output on 16-bit POD
- OC4-6 Pattern generator output on 8-bit POD

Note: The signal connector can also have other markings, like P1, U1, etc. Please refer to the POD-specific documentation for the signal connector name and signals present.

For every POD the following information is given:

- Ordering code. If there are different speed versions of a POD the ordering code is modified by appending the speed in MHz (IC81020-16 for the 16 MHz 8031 POD)
- information on available speed versions and required Emulator access time
- POD size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

Note: The In-Circuit Emulator can emulate a processor or a microcontroller. Beside the CPU, additional logic is integrated on the POD. The amount of additional logic depends on the emulated CPU and the type of emulation. A buffer on a data bus is always used (minimal logic) and when rebuilding ports on the POD, maximum logic is used. As soon as a POD is inserted in the target instead of the CPU, electrical and timing characteristics are changed. Different electrical and timing characteristics of used elements on the POD and prolonged lines from the target to the CPU on the POD contribute to different POD characteristics. Consequently, signal cross-talks and reflections occur, capacitance changes, etc.

Beside that, pull-up and pull-down resistors are added to some signals. Pull-up/pull-down resistors are required to define the inactive state of signals like reset and interrupt inputs, while the POD is not connected to the target. Because of this, the POD can operate as standalone without the target.

Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

For Better Understanding of the Hardware Reference: PIN 1 locations

There are several references to pin 1 in the manual and many jumper settings, CPU and pinout orientations rely on the correct location of pin 1. If sometimes the location of pin 1 is not clear, check the markings on the POD. If there are no markings, check the PCB board of the POD. Pin 1 is always marked on the PCB with a square pin (the other pins are round). The pin 1 location is also visible on the board in the hardware reference, if not any other way it can be identified by searching for the square pin.

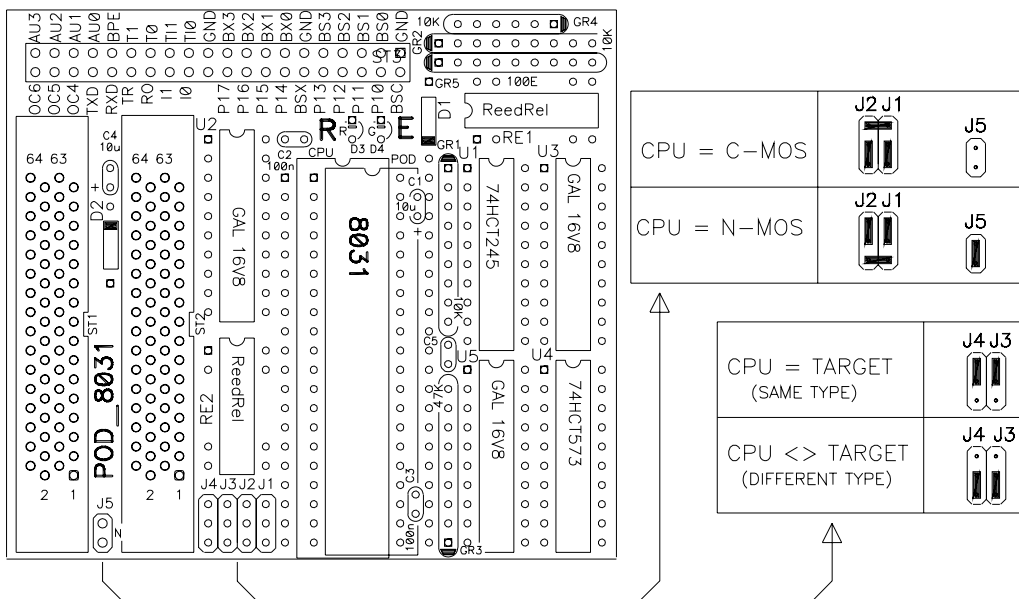
POD Hardware Reference

Intel 8031 POD rev. G

Ordering code	IC81020		
POD Speed (MHz)	16	24	42
Emulator Speed (ns)	150	90	65
Bank switch support	YES		
Exchange CPU	YES		
Dimensions (mm)	80x74		
Pin 1 position (mm)	41x52		

This POD can be used on iC181, iC1000 and the PowerEmulator unit.

Before connecting the PODs, make sure you have read the technical notes on Intel 8051 Family in the Hardware User's Guide.



Intel 8031 POD

Emulated CPU
8031, 80C31 - 8032, 80C32
8051, 80C51 (*) - 8052, 80C52 (*)
83C44
80C154 (*)
80C652 - 80C654
80C851
80C410
SAB-C501, SAB-C502

Note: CPUs with internal ROM (*) can only be used if P0 and P1 CPU ports are available for external mode addressing. In such case program that resides in internal ROM must be downloaded.

Jumper settings

Whenever the CPU is exchanged, the jumpers J1-J5 must be set according to CMOS/NMOS type of the CPU. See the jumper settings displayed next to the POD picture for settings.

Signal connector

A signal connector, marked ST3, is located on the POD.

Description	Signal	Pin	Pin	Signal	Description
Ground	GND	1	2	BSC	CODE Bank Size select. Open<=32k; Bridged=64k
Bank select line for CODE memory banking	BS0	3	4	P10	Port P1 output pin for bank switching
Bank select line for CODE memory banking	BS1	5	6	P11	Port P1 output pin for bank switching
Bank select line for CODE memory banking	BS2	7	8	P12	Port P1 output pin for bank switching
Bank select line for CODE memory banking	BS3	9	10	P13	Port P1 output pin for bank switching
Ground	GND	11	12	BSX	XDATA Bank Size select. Open<=32k; Bridged=64k
Bank select line for CODE memory banking	BSX0	13	14	P14	Port P1 output pin for bank switching
Bank select line for CODE memory banking	BSX1	15	16	P15	Port P1 output pin for bank switching
Bank select line for CODE memory banking	BSX2	17	18	P16	Port P1 output pin for bank switching
Bank select line for CODE memory banking	BSX3	19	20	P17	Port P1 output pin for bank switching
Ground	GND	21	22	n.c.	Not used
Target interrupt, bridge with I0 to enable interrupt	TI0	23	24	I0	Bridge with TI0 to enable target interrupt
Target interrupt, bridge with I1 to enable interrupt	TI1	25	26	I1	Bridge with TI0 to enable target interrupt
Timer output	T0	27	28	RO	Reset Output
Timer output	T1	29	30	TR	Target Reset Input
External Breakpoint input, active high	BPE	31	32	RXD	Receive line for serial channel 0
AUX signal input	AUX0	33	34	TXD	Transmit line for serial channel 0
AUX signal input	AUX1	35	36	OC4	Pattern Generator Output
AUX signal input	AUX2	37	38	OC5	Pattern Generator Output
AUX signal input	AUX3	39	40	OC6	Pattern Generator Output

ST3 signal connector pinout and description

Target POD Pinout

The target POD pinout is a standard DIP40.

Notes:

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