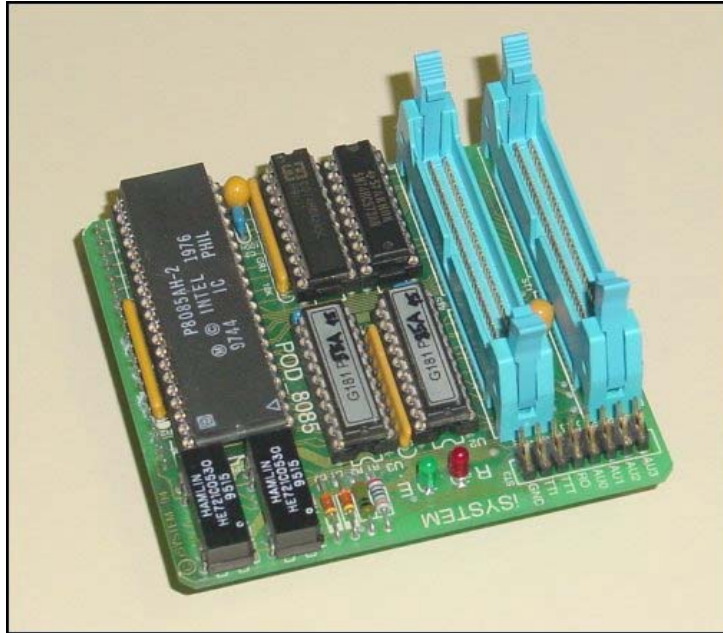

POD Hardware Reference**Intel 8085 POD Rev. A**

Ordering code	IC81014
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POD Hardware Reference

In-Circuit Emulation PODs

The following elements of interest are located on all In-Circuit emulation PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED (D3) - lit when CPU is running
- green LED (D4) - lit when Emulator is ready for emulation
- a connector, mostly marked ST3 - contains signal lines, some of which are hardware configuration lines (such as bank select signals), others you can use for signal generation (pattern generator outputs).

Here are some common signals found on the signal connector, commonly marked as ST3:

- GND Ground
- BPE External breakpoint input. Active high.
- RESO/RO Reset output. Connect to target to reset peripherals.
- TRES/TR Target reset input.
- AUXn AUX signal inputs (same as inputs on Emulator/trace)

Note: On PODs that support synchronization between two or more Emulators (currently only the HC(S)12 Family, see the Synchronization section in the Hardware User's Guide for more information) AUX0 and AUX1 are cut short with Run/Stop synchronization line, and AUX2, AUX3 with RESET synchronization line. You should use these pins to connect to other PODs or target CPUs.

- PAT0-2 Pattern generator output on 16-bit POD
- OC4-6 Pattern generator output on 8-bit POD

Note: The signal connector can also have other markings, like P1, U1, etc. Please refer to the POD-specific documentation for the signal connector name and signals present.

For every POD the following information is given:

- Ordering code. If there are different speed versions of a POD the ordering code is modified by appending the speed in MHz (IC81020-16 for the 16 MHz 8031 POD)
- information on available speed versions and required Emulator access time
- POD size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

Note: The In-Circuit Emulator can emulate a processor or a microcontroller. Beside the CPU, additional logic is integrated on the POD. The amount of additional logic depends on the emulated CPU and the type of emulation. A buffer on a data bus is always used (minimal logic) and when rebuilding ports on the POD, maximum logic is used. As soon as a POD is inserted in the target instead of the CPU, electrical and timing characteristics are changed. Different electrical and timing characteristics of used elements on the POD and prolonged lines from the target to the CPU on the POD contribute to different POD characteristics. Consequently, signal cross-talks and reflections occur, capacitance changes, etc.

Beside that, pull-up and pull-down resistors are added to some signals. Pull-up/pull-down resistors are required to define the inactive state of signals like reset and interrupt inputs, while the POD is not connected to the target. Because of this, the POD can operate as standalone without the target.

Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

For Better Understanding of the Hardware Reference: PIN 1 locations

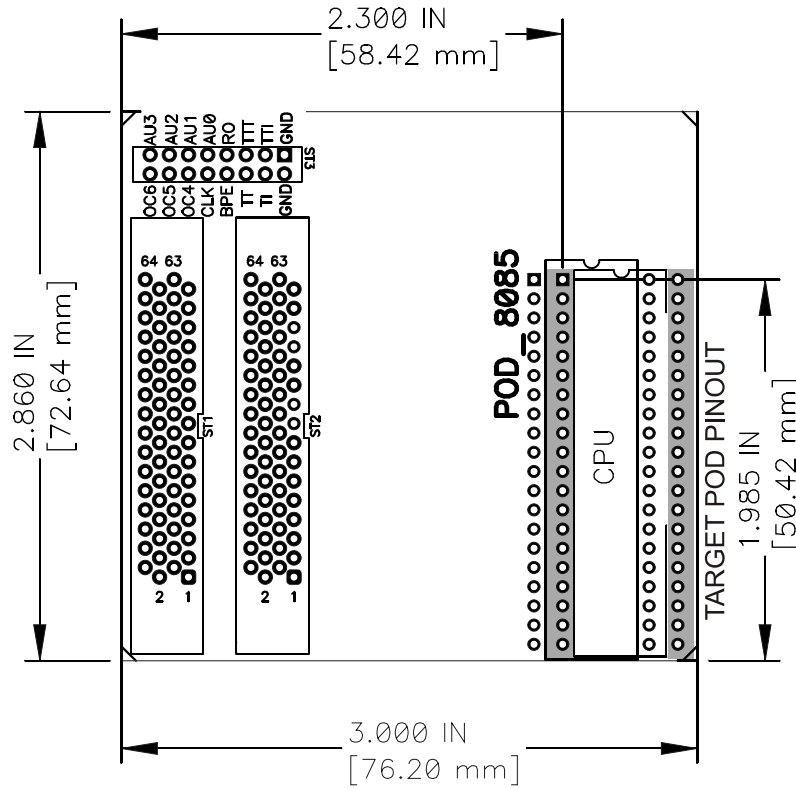
There are several references to pin 1 in the manual and many jumper settings, CPU and pinout orientations rely on the correct location of pin 1. If sometimes the location of pin 1 is not clear, check the markings on the POD. If there are no markings, check the PCB board of the POD. Pin 1 is always marked on the PCB with a square pin (the other pins are round). The pin 1 location is also visible on the board in the hardware reference, if not any other way it can be identified by searching for the square pin.

POD Hardware Reference

Intel 8085 POD Rev. A

Ordering code	IC81014
POD Speed (MHz)	6
Emulator Speed (ns)	90
Dimensions (mm)	76x72
Pin 1 position (mm)	60x50

Before connecting the PODs, make sure you have read the technical notes on the Intel 8085 Family in the Hardware User's Guide.



Top POD View

Emulated CPU
8085

The Signal Connector

A signal connector is present on this pod, marked as ST3.

Description	Signal	Pin	Pin	Signal	Description
Pattern Generator Output	OC6	16	15	AU3	AUX Input
Pattern Generator Output	OC5	14	13	AU2	AUX Input
Pattern Generator Output	OC4	12	11	AU1	AUX Input
CPU signal for monitoring	CLK	10	9	AU0	AUX Input
External Breakpoint	BPE	8	7	RO	Reset Output
Bridge to TTT to enable Target Trap	TT	6	5	TTT	Bridge to TT to enable Target Trap
Bridge to TTI to enable Target Interrupt	TI	4	3	TTI	Bridge to TI to enable Target Interrupt
Ground	GND	2	1	GND	Ground

ST3 Connector signals

Pull-up and pull-down lines

- HOLD, INTR, RST55, RST65, RST75, TRAP and RESET signals have a 10k pull-down on the POD.
- RD, IOM and READY signals have a 10k pull-up on the POD.
- WR is connected through GAL because it has to be non-active when the CPU is running in monitor.
- The data signals are connected through a 245 buffer.
- All other signals are connected directly (if jumpers for INTR and TRAP are inserted).

Common Issues

Clock

Clock source can be either used internal from the emulator or external from the target. It is recommended to use the internal clock when possible. When using the clock from the target, it may happen that the emulator cannot initialize any more.

It is dissuaded to use a crystal in the target as a clock source during the emulation. It is recommended that the oscillator is used instead. Normally, a crystal and two capacitors are connected to the CPU's clock inputs in the target application as stated in the CPU datasheets. A length of clock paths is critical and must be taken into consideration when designing the target. During the emulation, the distance between the crystal in the target and the CPU (on the POD) is furthermore increased, therefore the impedance may change in a manner that the crystal doesn't oscillate anymore. In such case, a standalone crystal circuit, oscillating already without the CPU must be built or oscillator used.

Checksum

When performing any kind of checksum in the emulated (code) area, note that all breakpoints must be removed before, otherwise the results are distorted. Note that the emulator forces "breakpoint" instruction on the data bus when executing the code at the address where breakpoint is set.

Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch,...) to eliminate any possible influence of the emulator on the CPU execution.

There were cases where the target application was behaving differently with the target CPU inserted or the POD connected.

If the the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly as the peripheral device was not configured properly.

Target POD Pinout

The target POD pinout is the standard DIP40.

Notes:

Notes: