
POD Hardware Reference

MC9S12 Expanded ActivePOD

Ordering code	IC30405
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POD Hardware Reference

Active POD

Active PODs

Active PODs can be used connected to iC3000(HS) or iC4000 Emulator through the iBUS Active Emulator/Trace interface.

The following elements of interest are located on all Active PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED - lit when CPU is running
- green LED - lit when Emulator is ready for emulation

For every POD following information is given:

- ordering code;
- information on available speed versions and required Emulator access time;
- size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

PIN1 location on every component is also marked on the circuit board with a square block (PIN 1 pin is soldered a square block, other pins have a round pin).

Trace

The ActivePOD has integrated Trace capabilities that can be utilised if the interface iCard with trace capabilities is used. See the Trace section in the Hardware User's Guide for general information on Trace and POD information for specific information on trace signals (AUX, TrigOut, etc.).

Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

POD Hardware Reference

ActivePOD Emulator Unit II

Ordering code	IC30250
Board dimensions (mm)	98x82



This Emulator Unit is used on some ActivePODs and is used with an ActiveEmulator II iCard.

The following elements of interest are located on the Emulator Unit:

- Green LED LD1 - Emulation - lit when Emulator is ready for emulation
- Red LED LD2 – Running – lit when CPU is running
- LD3 – CPU Power LED – lit when the CPU is powered (either when the POD is not connected to a target or is connected to the target and the target power supply is on)
- LD4 – POD Power LED – lit when the Emulator is powered

The Emulator unit has a Target connector with the following signals:

19	17	15	13	11	9	7	5	3	1
AUX1	AUX3	AUX5	AUX7	AUX9	AUX11	AUX13	AUX15	TRIGOUT	GND
AUX0	AUX2	AUX4	AUX6	AUX8	AUX10	AUX12	AUX14	EXTBP	GND
20	18	16	14	12	10	8	6	4	2

- AUX0 – 15 – available AUX inputs (3V LVTTL, connected to FPGA)

Note: The number of AUX inputs depends of the ActivePOD.

- TrigOut – Trigger or Qualifier output (depending on the setting in the Trigger dialog), active low, when trigger condition occurred (3V LVTTL, connected to FPGA)

The Trigger output is approx. 160µs wide.

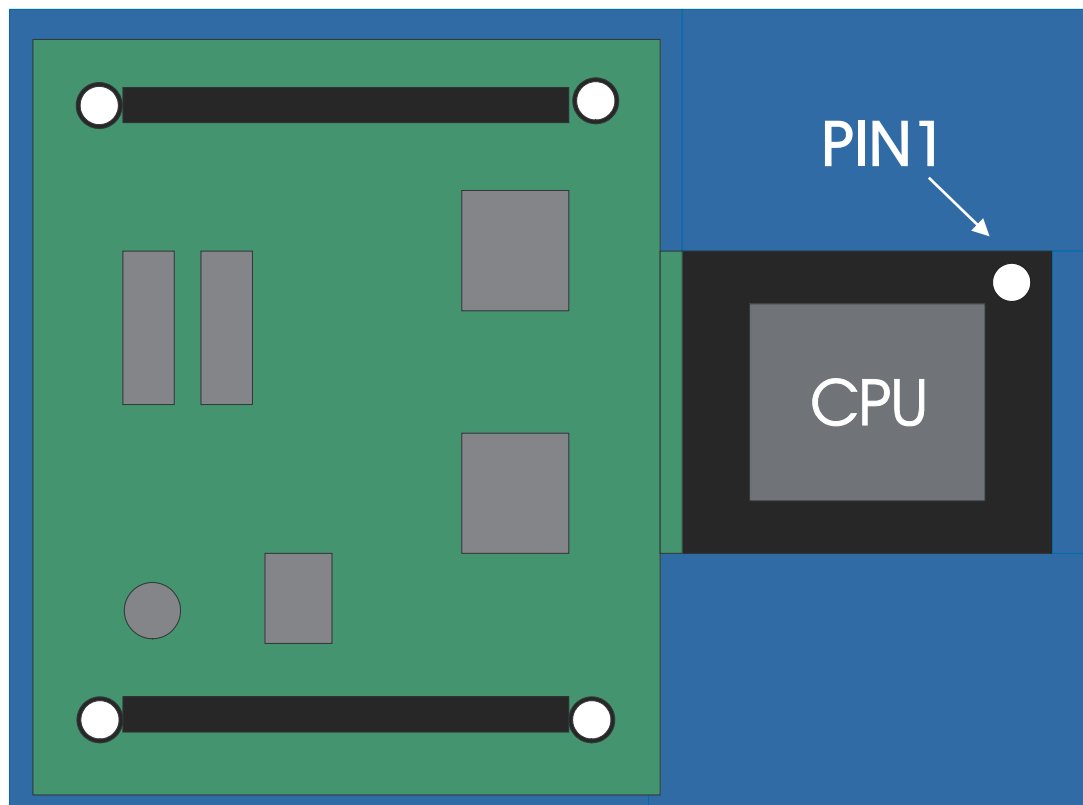
POD Hardware Reference

MC9S12 Expanded ActivePOD

Ordering code	IC30405
POD ECLK Speed (MHz)	25
Exchange CPU	YES
Trace Depth	128k
Board dimensions (mm)	99x123
Pin 1 position (mm)	71x118

This POD is connected to the ActivePOD Emulator Unit II.

Before connecting the PODs, make sure you have read the technical notes on Motorola 68HC12 Family in the Hardware User's Guide.



ActivePOD

Emulated CPUs	
MC9S12B256	MC9S12B128
MC9S12B64	MC9S12C128
MC9S12C96	MC9S12C64
MC9S12C32	MC9S12A64
MC9S12A256	MC9S12A128
MC9S12D32	MC9S12DB32
MC9S12D64	MC9S12DJ64
MC9S12DB128	MC9S12DG128
MC9S12DJ128	MC9S12DT128
MC9S12DG256	MC9S12DJ256
MC9S12DP256	MC9S12DT256
MC9S12DP512	MC9S12KG128
MC9S12KT256	

Note: The list of emulated CPUs is very dynamic and is only valid at the time of creation of this document. For the latest list of supported devices, please check the iSYSTEM web page.

This ActivePOD is connected to the ActivePOD Emulation Unit II and this unit is connected to the Emulator with an iCARD ActiveEmulator II interface. Do not use the ActiveEmulator I iCard.

POD Features

This POD is specifically designed for expanded mode emulation. Single-chip emulation is not possible with this POD, since no overlay memory is present and the program runs from the CPU FLASH. Because of the same reason, synchronization of two or more emulators is not possible.

The POD features two hardware and an unlimited number of FLASH software breakpoints. Access breakpoints are available, but task breakpoints are not.

The FLASH life cycle is around 10.000 programmings.

The trace, code coverage and profiler are also available.

To reach exact CPU timings, no emulation memory is present on the POD. There are no buffers for addresses and no buffers for data. All ports, address and data lines except MODA and MODB are connected directly from the CPU to target. The MODA and MODB lines are connected through digital switches (propagation delay 0.3ns when open). These switches are closed during reset, so that the emulator is able to start the emulation in single chip special mode, after that it switches to the mode selected in winIDEA.

To run the code, the emulator (CPU) is using internal FLASH or external RAM. Internal flash is selected by the option 'Use internal FLASH for emulation'. When this option is selected, internal FLASH is programmed during download. For FLASH programming the emulator is using a monitor, loaded to internal FLASH. Be sure that the correct CPU is selected because internal RAM position and the size of it depends on the CPU. When the option 'Use internal FLASH for emulation' is enabled, only internal FLASH is programmed during download.

If any code must to be loaded to RAM or EEPROM, target download must be used.

Breakpoints

The POD supports two types of breakpoints:

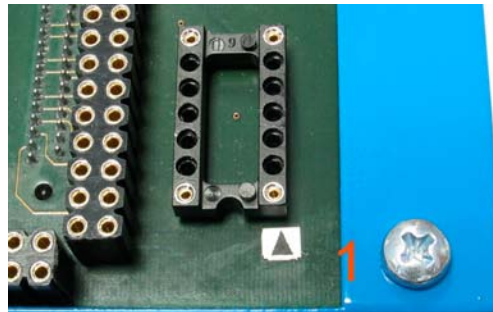
- Hardware breakpoints
- Emulator (software) breakpoints

When using software breakpoints in the internal FLASH, please note, that the FLASH is programmed every time a breakpoint is inserted or removed. Be careful when using these breakpoints because the maximum number of programming cycles (approx. 10.000) can expire.

Clock Setting

Selecting in winIDEA™, the POD can use either internal or external clock from the target.

When internal clock is selected, the user can choose the clock from the emulator (marked as PLL) or a clock generated by the inserted oscillator (Q1) on the bottom side of the POD (see picture below). A jumper J4 on the bottom side of the POD selects internal clock source being used. An operating frequency is set in the winIDEA™, when using a clock from the emulator. When inserted oscillator is used, it must have 5V voltage levels even though the CPU requires 2.5V levels. 5V oscillator output is divided down to necessary 2.5 V by the POD.



Q1 Pin 1 location

J4 setting	Internal clock source
1-2 (*)	PLL (emulator)
2-3	Q1 Oscillator

Jumper J4 settings (- factory default)*

Note that Pin 1 on the J4 jumper is marked with an arrow, and Pin 1 of the Q1 Oscillator is also marked with an arrow.

When external clock is selected, the POD uses a clock from the target. Motorola has defined very precise PCB and connection guidelines when using a crystal as a clock source. Since these guidelines cannot be considered on the POD completely, it's not recommended to use a crystal in the target as a clock source. The distance between the crystal in the target and the CPU on the POD is critical and thus the crystal may not oscillate at all. Therefore, when external clock is being used, it is recommended to use an oscillator in the target to assure initialization and operation of the system. The oscillator used in the target must be 2.5V type, as the CPU requires 2.5V clock.

The CPU has the XCLKS pin, with which the type of oscillator (depending on the hardware implementation of the oscillator circuit) used is selected during reset, and either the Full swing Pierce oscillator / external clock source or a Loop controlled Pierce oscillator can be selected. The XCLKS pin is connected directly from CPU to target, therefore it is the user's responsibility to drive this pin correctly. For more information on both types of oscillators, please consult the CPU manual.

A pulldown should be connected to XCLKS when MC9S12KG128 or MC9S12KT256 devices are on the POD but the POD is not inserted into the target.

Vcc Setting

Vcc selection (Internal/External) in winIDEA™ is ignored at this particular POD. The CPU ports operate at 5V always. 5V power supply for the CPU ports is always supplied from the emulator, regardless whether the POD is connected to the target or not. However, internal CPU core operates at 2.5V. This voltage can be generated internally by the CPU, using internal regulator, or external voltage can be used. Which voltage is being used, depends on the state of the CPU's VREGEN pin.

When the POD is not connected to the target, the CPU core uses internally generated voltage.

When the POD is connected to the target, the CPU senses the VREGEN (Voltage Regulator Enabled) pin to determine whether the internal voltage regulator is active and used or the power supply from the target is used. When using external power supply (VCCPLL, VCC1, VCC2), Motorola's guidelines must be considered.

Target connection detection

By default, the emulation system auto-detects whether the POD is connected to the target or not and supplies the power to the sensitive POD logic only while the target is switched on. Consequentially, optimum conditions are met since the POD is powered synchronously to the target. In worst case, wrong manual switch on/off order can damage the hardware. Debug download is not possible while the POD is connected to target being switched off.

The auto-detection can be turned off using the J4 jumper.

J4 setting	Auto-detection
Set (*)	Auto-detection enabled
Removed	Auto-detection disabled

Jumper J4 settings (- factory default)*

If the auto-detection is disabled, the emulator doesn't auto detect whether the target is powered or not and supplies the power to the POD logic when the emulation system is switched on. The debug download is possible even while the target is switched off.

AUX inputs

This ActivePOD supports 4 AUX inputs. The connector is available on the Emulation unit. Note that on the Emulation Unit II, AUX0 to AUX3 are active only. Any digital signal connected to the AUX input can be recorded by the analyzer, operating in the trace mode. Trigger on it can be set as well.

Emulating MC9S12C32/C64/C96/C128

MC9S12C derivatives have minor differences comparing to other MC9S12 derivatives. When emulating them, pay attention that the C128 (96,64,32) must be selected in winIDEA

Known CPU design flaw (MC9S12C128, mask 0L09S and MC9S12B128)

Internal RAM is disabled after reset. To enable it, INITRM register must be written prior any write to the internal RAM.

COP troubleshooting

When using COP, 'Reset from Target enabled' option in winIDEA 'CPU Setup/Options' dialog must be checked. When COP reset is generated, the CPU drives reset line. Any "non emulator" reset is target reset.

Using COP

The CPU has an internal watchdog, that must be refreshed periodically, or the CPU resets. The COP can be disabled in STOP (while the CPU is stopped by BDM), which is necessary for debugging. Since the register, which turns off COP is a write-once register, the whole register must be written.

Using COP with Star12 PODs

Use COP is a global option with, which the COP usage is selected. If this option is enabled, the option to insert COPCTL is available. If COP is enabled, the software presets the COPCTL register (address 0x003C) with the value, entered into the COPCTL field. It makes sure automatically that RSBCK (the bit, that disables COP while the user program is stopped) is always active.

Target (Watchdog) Reset and Assume Target Reset

If COP is enabled, the 'Target RESET Enabled' function must be enabled. At COP reset the CPU forces a reset, that the emulator only recognizes as target reset.

The Star12 CPUs have three sorts of resets with each having its own individual vector. These are:

- External reset - power on. Vector 0xFFFFE-0xFFFF
- Clock monitor fail reset. Vector 0xFFFFC-0xFFFFD
- COP failure reset. Vector 0xFFFFA-0xFFFFB

In most cases all vectors point to the same location, but this does not have to be so.

To test the situation when the program starts after reset with another vector, the software has three 'Assume Target RESET' options:

- Other (default) (Vector 0xFFFFE-0xFFFF)
- Clock monitor fail (Vector 0xFFFFC-0xFFFFD)
- COP failure (Vector 0xFFFFA-0xFFFFB)

Depending on the selected option, the CPU starts at every target reset on the location, to, which the appropriate vector points.

At every emulator reset (through the software) the CPU always starts on the location, to, which the 0xFFFFE-0xFFFF vector is pointing.

Emulation Mode

The Emulation Mode in which the POD operates can be set in the software. Two operating modes are available:

- Expanded Wide Mode (16-bit)
- Expanded Narrow Mode (8-bit)

The Port E Assignment Register

The value which is written to the CPU PEAR register after any reset must be specified in the Advanced CPU options dialog. Be sure that all external signals which are used in the target (ECLK, LSTRB, RW) are enabled or disabled correctly.

Note: Trace on the POD requires PIPE signals for program flow reconstruction. PIPE signals are enabled by PIPOE bit in PEAR register. Be sure that this bit is set if you want to use the trace.

General HC12 Emulation Notes

Clock

There are two major issues the user must pay attention to when using external clock:

- Also when using external clock, the user must specify target clock frequency ($2 \cdot \text{ECLK}$) in the 'Hardware/Emulation Options/Vcc/Clock' tab, like in the case when using internal clock. It is required by the debugger to be able to synchronize with on-chip BDM firmware which operates at CPU's system clock frequency.
- It is not recommended to use a crystal in the target as a clock source during the emulation. It is recommended that the oscillator is used instead. Normally, a crystal and two capacitors are connected to the CPU's clock inputs in the target application as stated in the CPU datasheets. A length of clock paths is critical and must be taken into consideration when designing the target. During the emulation, the distance between the crystal in the target and the CPU (on the POD) is furthermore increased, therefore the impedance may change in a manner that the crystal doesn't oscillate anymore. In such case, a standalone crystal circuit, oscillating already without the CPU must be built or oscillator used.

COP

COP is fully supported, unless DP256 mask 0K36N is used. It is not advisable to use this mask of the CPU, since also other problems can arise. If the DP256 with the mask 0K36N must be used, select the 'DP256 Rev I' CPU in winIDEA. In this case, COP is not supported due to CPU specifics. If this mask is used, internal COP must be disabled when using the emulator, respectively while debugging.

When experiencing some problems with the emulator when using COP, please check, whether you have correct/valid interrupt vector table. If some other interrupt vector is defined by mistake as a watchdog interrupt vector, it may look like the COP resets the CPU when the interrupt occurs.

STOP Instruction

The STOP instruction is not supported because this instruction also causes the BDM to stop.

Internal RAM, Internal EEPROM

HCS12 derivatives don't allow writing to the internal EEPROM area via single memory access. They require an EEPROM programming algorithm, which is also implemented in winIDEA. The user can download to the EEPROM and modify its content in the memory window.

Considerations:

- 1) After reset, the EEPROM area is on some CPUs (e.g. MC9S12DP256) covered with the I/O area, the priority of which is higher than the priority of EEPROM and thus the EEPROM or portion of it may not be available.
- 2) The CPU has an EEPROM Protection Register (EEPROT). By this register, a certain EEPROM block can be protected. If a certain block is protected, the emulator and the user's program cannot change its content.
- 3) The CPU has an ECLKDIV register with which the EEPROM clock is set. The register contains division factor set according to the CPU specifications (EEPROM clock frequency of 150-200kHz is required). The emulator does not write to this register.

To download a file to the internal EEPROM:

- 1) 'Target Download' must be used;
- 2) The ECLKDIV register must be set using the initialization sequence;

- 3) If the whole EEPROM is required, the EEPROM area must be relocated with the initialization sequence (by writing to the INITEE register). This is necessary because on some CPUs the EEPROM area is covered with the I/O area. Don't forget to set a proper offset for the download file when relocating EEPROM memory area.
- 4) The EEPROM writes must not be disabled.

The run, stop and single step debug commands can be used in the internal RAM or EEPROM. Single step can be performed either in the disassembly or source window. Breakpoints can be set as well.

PLL

The Active PODs support PLL use.

After the PLL is initialized, below equation defines new CPU system clock frequency:

1) after reset PLL is inactive

$Extal = 2 * ECLK$

2) PLL enabled

$ECLK = Extal * (SYNR + 1) / (REFDIV + 1)$

Checksum

When performing any kind of checksum in the emulated (code) area, note that all breakpoints must be removed before, otherwise the results are distorted. Note that the emulator forces "breakpoint" instruction on the data bus when executing the code at the address where breakpoint is set.

Slow Mode

It is not recommended to debug the application running in slow mode, due to a CPU flaw.

'Clear on read' register bits

Be careful when the CPU has register bits that are cleared on read access. Do note that when such register (memory location) is accessed either by memory/watch window or SFR window, the flags are cleared and the application may behave different when using the emulator or the target CPU. It is recommended not to display such register or the associated memory location in the memory/watch window during final test. Otherwise, it may happen that the target application doesn't work due to the bug in the code even though it works with the emulator.

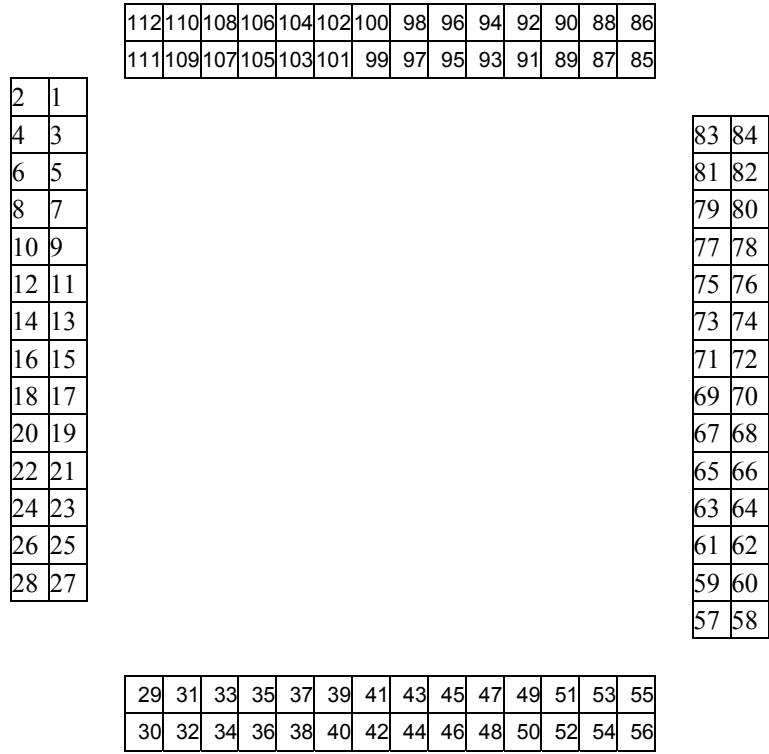
For instance, the user makes a mistake and doesn't clear the flag in the application. Using the emulator, the application works correctly since the user uses SFR window which clears the flag when the window is updated.

Target Adapters

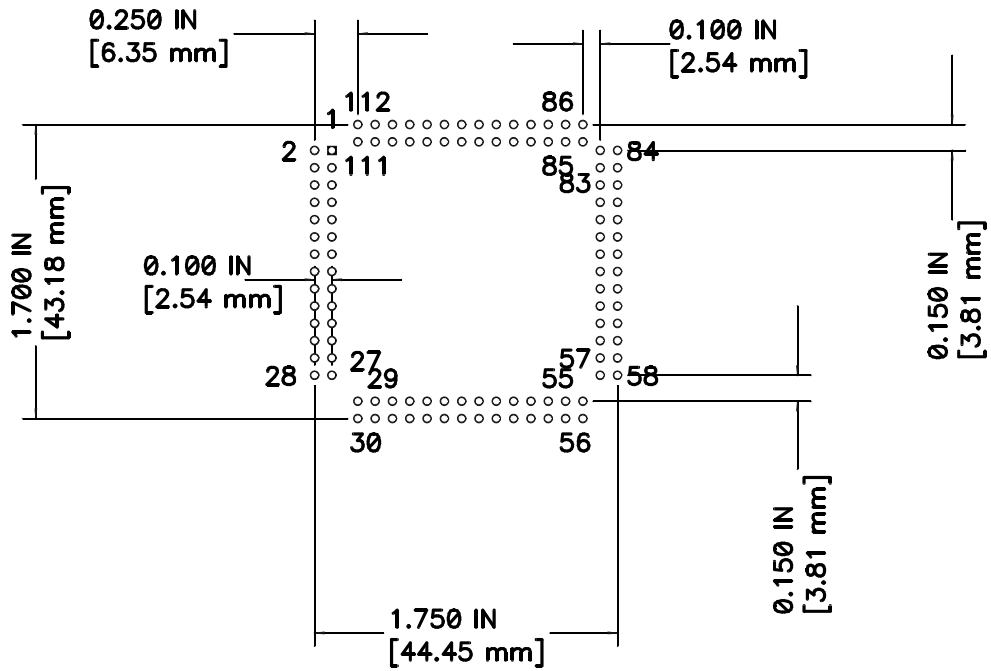
iSYSTEM offers various adapter solutions for this POD. Please refer to the adapter documentation for more details.

POD Target Layout

The POD target layout is T_QFP112.



T_QFP112 – Top POD view



T_QFP112 Dimension

Notes: