
POD Hardware Reference

MC9S12HZ256 ActivePOD II Rev. B

Ordering code	IC30408
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POD Hardware Reference

Active POD

Active PODs

Active PODs can be used connected to iC3000(HS) or iC4000 Emulator through the iBUS Active Emulator/Trace interface.

The following elements of interest are located on all Active PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED - lit when CPU is running
- green LED - lit when Emulator is ready for emulation

For every POD following information is given:

- ordering code;
- information on available speed versions and required Emulator access time;
- size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

PIN1 location on every component is also marked on the circuit board with a square block (PIN 1 pin is soldered a square block, other pins have a round pin).

Trace

The ActivePOD has integrated Trace capabilities that can be utilised if the interface iCard with trace capabilities is used. See the Trace section in the Hardware User's Guide for general information on Trace and POD information for specific information on trace signals (AUX, TrigOut, etc.).

Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

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ActivePOD Emulator Unit II

Ordering code	IC30250
Board dimensions (mm)	98x82



This Emulator Unit is used on some ActivePODs and is used with an ActiveEmulator II iCard.

The following elements of interest are located on the Emulator Unit:

- Green LED LD1 - Emulation - lit when Emulator is ready for emulation
- Red LED LD2 – Running – lit when CPU is running
- LD3 – CPU Power LED – lit when the CPU is powered (either when the POD is not connected to a target or is connected to the target and the target power supply is on)
- LD4 – POD Power LED – lit when the Emulator is powered

The Emulator unit has a Target connector with the following signals:

19	17	15	13	11	9	7	5	3	1
AUX1	AUX3	AUX5	AUX7	AUX9	AUX11	AUX13	AUX15	TRIGOUT	GND
AUX0	AUX2	AUX4	AUX6	AUX8	AUX10	AUX12	AUX14	EXTBP	GND
20	18	16	14	12	10	8	6	4	2

- AUX0 – 15 – available AUX inputs (3V LVTTL, connected to FPGA)

Note: The number of AUX inputs depends of the ActivePOD.

- TrigOut – Trigger or Qualifier output (depending on the setting in the Trigger dialog), active low, when trigger condition occurred (3V LVTTL, connected to FPGA)

The Trigger output is approx. 160µs wide.

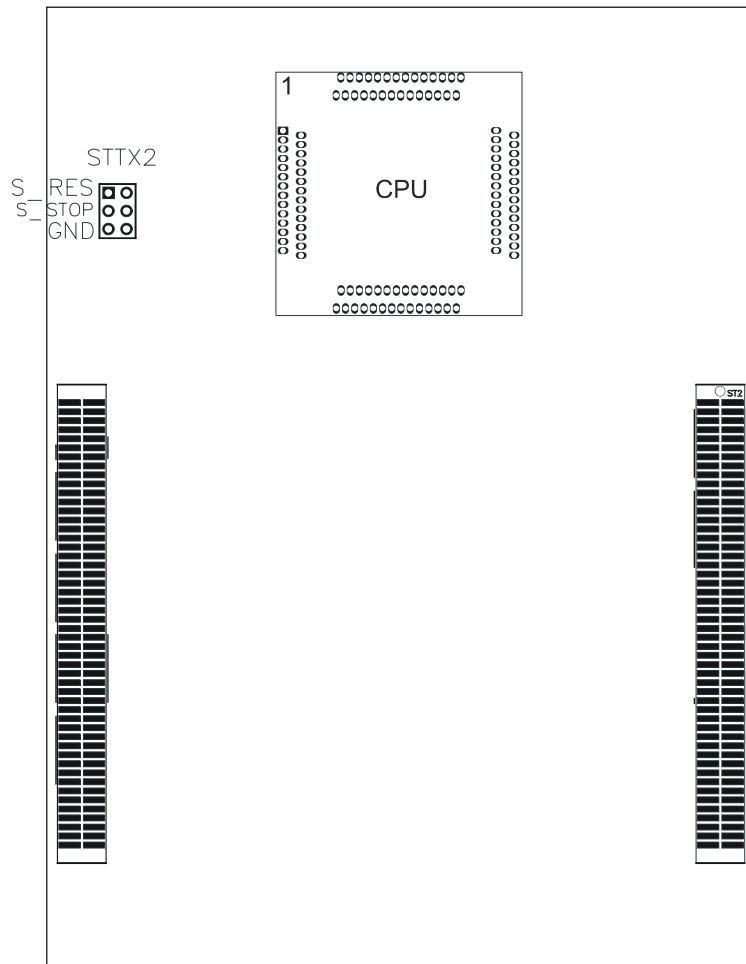
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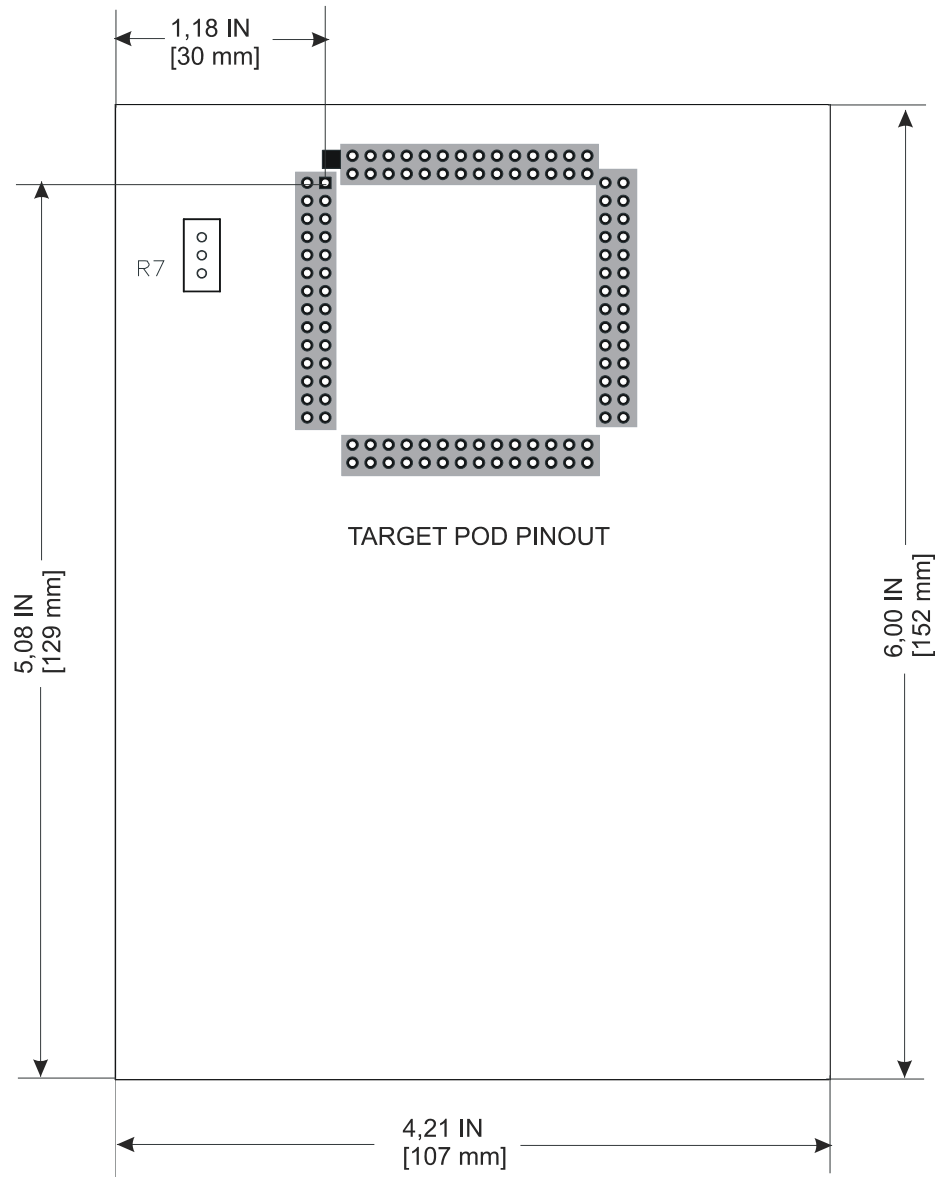
Ordering code	IC30408
POD ECLK Speed (MHz)	25
Exchange CPU	YES
Trace Depth	128k

This POD is connected to the ActivePOD Emulator Unit II.

Before connecting the PODs, make sure you have read the technical notes on Motorola 68HC12 Family in the Hardware User's Guide.



ActivePOD Top Board



ActivePOD Bottom Board

Emulated CPU
MC9S12HZ128
MC9S12HZ256

This ActivePOD is connected to the ActivePOD Emulation Unit II and this unit is connected to the Emulator with an iCARD ActiveEmulator II interface. Do not use the ActiveEmulator I iCard.

Emulation and electrical differences

This POD emulates the MC9S12HZ256 CPU in Single Chip Mode. The CPU internally contains 256KB of FLASH and has an integrated LCD controller, which is able to control up to 128 (32x4) LCD segments. The LCD controller shares the ports with digital I/O ports.

The POD emulates the Single Chip Mode, but the CPU on the POD operates in Expanded Wide Mode. For proper operation of the POD, the ECLK, RW, LSTRB, Pipe0 and Pipe1 signals are required.

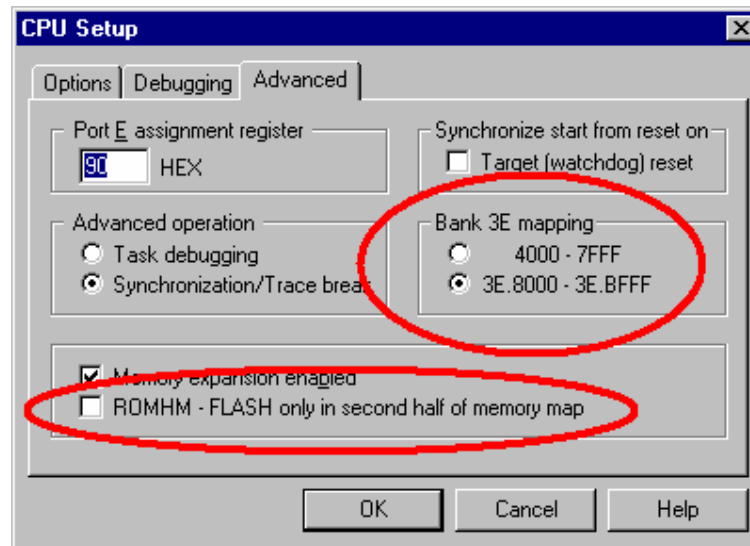
The CPU on the POD operates in the expanded mode, but it behaves to the target as operating in the single chip mode. Since the CPU on the POD operates in the expanded mode while emulating the single chip mode, some registers, like PEAR and MODE, contain different values than expected by the user. In addition, they cannot be written by the user. PEAR register value used by the application must be written in the debugger's 'Advanced' dialog. PEAR register cannot be written by the application itself.

Because the LCD controller shares its pins with pins of Port A, Port B and Port E with Address/Data and Control Bus, a special circuit is required on the POD to reconstruct the LCD controller.

The program scheme of the program memory is identical to the scheme of the internal FLASH:

- common area from 0xC000 to 0xFFFF, also available as Bank 0x3F,
- bank area from 0x8000 to 0xBFFF, altogether 16 banks,
- common area from 0x4000 to 0x7FFF, also available as Bank 0x3E.

The area between 0x4000 and 0x7FFF can be used in various ways. The basic usage is having this area also mapped to the Bank 0x3E area. The usage of this area must be specified in the software in the CPU Setup/Advanced dialog.



CPU Setup, Advanced dialog

The alternate usage is not using the 0x4000 area at all. This mode is selected with the ROMHM option (ROM available only in the upper memory area – from 0x8000).

General HC12 Emulation Notes

Clock

When using the external clock, the HC(S)12 application doesn't start. It works fine when I use internal clock. There are two major issues the user must pay attention to:

- Also when using external clock, the user must specify target clock frequency ($2 * ECLK$) in the 'Hardware/Emulation Options/Vcc/Clock' tab, like in the case when using internal clock. It is required by the debugger to be able to synchronize with on-chip BDM firmware which operates at CPU's system clock frequency.
- It is not recommended to use a crystal in the target as a clock source during the emulation. It is recommended that the oscillator is used instead. Normally, a crystal and two capacitors are connected to the CPU's clock inputs in the target application as stated in the CPU datasheets. A length of clock paths is critical and must be taken into consideration when designing the target. During the emulation, the distance between the crystal in the target and the CPU (on the POD) is furthermore increased, therefore the impedance may change in a manner that the crystal doesn't oscillate anymore. In such case, a standalone crystal circuit, oscillating already without the CPU must be built or oscillator used.

COP

Internal COP must be disabled when using the emulator, respectively while debugging

STOP Instruction

STOP instruction is completely supported by the emulator. After the STOP instruction is being executed, the CPU is stopped and the debugger displays HALTED status. Note that the debug windows cannot be updated while HALTED status is displayed. When the CPU is awoken either by interrupt or target reset, the emulation/execution proceeds normally.

Internal CPU Flash

Note that internal FLASH is disabled during the emulation and cannot be used in any way.

Internal RAM, Internal EEPROM

If the CPU provides a capability to write to the internal RAM or EEPROM via memory window (no specific programming sequence required), the download file can be loaded to the internal RAM or EEPROM using the 'Target Download' option. The debugger downloads the code to the internal memory after reset via the CPU. If the CPU requires some registers to be configured before the CPU is able to write into the EEPROM area, the user must configure the necessary registers respectively, using the initialization dialog. Any sequence, added in the initialization dialog, is executed immediately after reset, before the download is performed.

Executing the program in the internal RAM or EEPROM has some limitation, depending on the emulation system.

The run, stop and single step debug commands can be used in the internal RAM or EEPROM. Single step can be performed either in the disassembly or source window. Breakpoints can be set as well.

Note that HCS12 (MC9S12DP256, MC9S12H256,...) derivatives don't allow writing to the internal EEPROM area via memory window since a special programming sequence is required. Consequently, the download file cannot be loaded to the internal EEPROM by the debugger. Therefore, the programming algorithm must be implemented by the user in his application. Refer to the CPU datasheets for more details.

PLL

The Active PODs support PLL use.

After the PLL is initialized, below equation defines new CPU system clock frequency:

1) after reset PLL is inactive

$$\text{Extal} = 2 * \text{ECLK}$$

2) PLL enabled

$$\text{ECLK} = \text{Extal} * (\text{SYNR} + 1) / (\text{REFDIV} + 1)$$

Checksum

When performing any kind of checksum in the emulated (code) area, note that all breakpoints must be removed before, otherwise the results are distorted. Note that the emulator forces "breakpoint" instruction on the data bus when executing the code at the address where breakpoint is set.

Limitations

While the Register area in the CPU (including the Ports) can be freely moved, with the POD this area can only be moved to an address lower than 0x7FFF.

Note: This type of CPU does not allow the NECLK bit in the PEAR register to be locked. The Emulator requires the ECLK signal for its operation. Since the NECLK bit is not locked, the user can disable ECLK and the emulation would fail in this case – the emulator would report the "HALTED" status.

Vcc Setting

Vcc selection (Internal/External) in winIDEA™ is ignored at this particular POD. The CPU ports operate at 5V always. 5V power supply for the CPU ports is always supplied from the emulator, regardless whether the POD is connected to the target or not. However, internal CPU core operates at 2.5V. This voltage is generated internally by the CPU using an internal regulator.

Power Supply Sensor

A special logic is available in the POD to sense whether the POD is connected to the target or not. The sensor is created by checking the GND signal from pin 132 and the TVCC voltage from pin 50. As GND sense a pullup is generated, and as TVCC sense a pulldown is generated. The logic on the POD requires a high level from at least one of these two pins. When the POD is operating standalone, the GND sense signal is high (because of pullup) and low, when inserted into the target. The TVCC sense signal is expected to be high when the POD is connected to the target and low (because of the pulldown) when the POD is operating standalone.

The LCD Module

The LCD Module is built in two parts. The first part is a digital part of the controller, which is implemented in Xilinx and controls the analog part (the analog switches), which is connected directly to the LCD. The LCD controller can control up to 32 segments, that can be multiplexly organized. The LCD controller supports the multiplexes of 1, 2, 3 or 4, which means that a maximum of 128 (32x4) segments can be controlled at once.

The output levels of analog voltages depend on the multiplex and its values can be:

- 0V
- 1/3 VLCD
- 1/2 VLCD
- 2/3 VLCD
- VLCD

VLCD is the LCD power supply voltage. By changing the voltage of the LCD the brightness and the contrast of the LCD display are determined. A jumper J2 is available on the POD to select the VLCD power supply source.

J2 setting	VLCD Power Supply Source
1-2 (*)	Emulator
2-3	Target

Jumper J2 settings (- factory default)*

When VLCD is used from the emulator, its level can be set using the R7 potentiometer, located on the side of the POD. If VLCD is used from the target, the VLCD must be set in the target.



On the bottom board, connector J1 is available. Here, the VLCD voltage can be measured.

Pin	Description
1	VLCD
2	GND

Connector J1 (on the bottom board) pinout

AUX inputs

This ActivePOD supports 4 AUX inputs. The connector is available on the Emulation unit. Note that on the Emulation Unit II, AUX0 to AUX3 are active only. Any digital signal connected to the AUX input can be recorded by the analyzer, operating in the trace mode. Trigger on it can be set as well.

Synchronization of Two or More Emulators

When multiple emulators should operate synchronously, synchronization connector available on the side of the emulator, marked STTX2 must be used. All the emulators that should operate synchronously must have connected together (separately) SR (SYNC-RESET) pins, SS (SYNC-STOP) pins and GND (ground) pins.

2	4	6
GND	S-STOP	S-RESET
GND	S-STOP	S-RESET
1	3	5

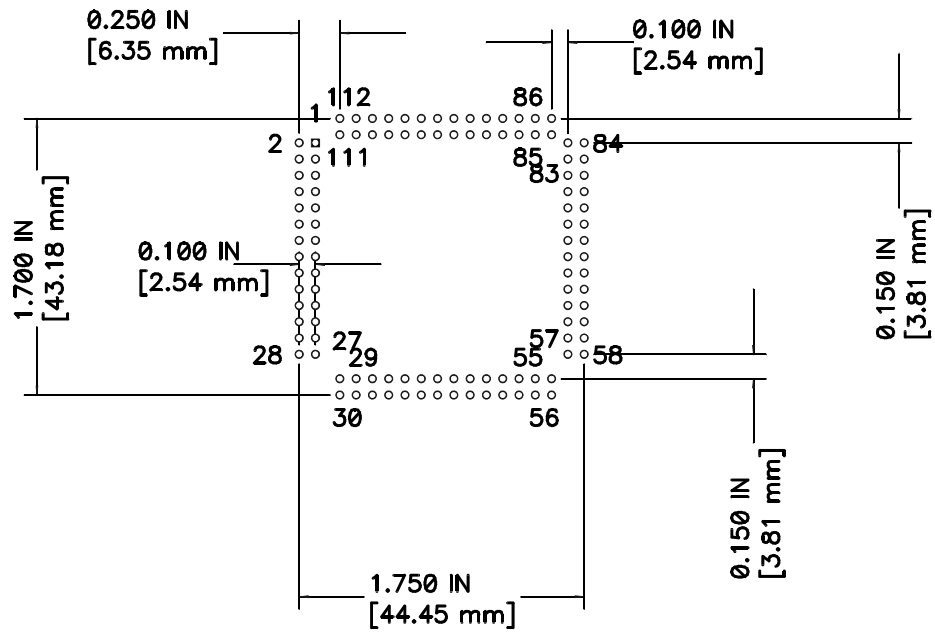
Synchronization connector STTX2

Two lines for each signal are present to allow easier connection of multiple Emulators.

For more information, please refer to the "Synchronization of Two or More Emulators" section of the Hardware User's Guide.

Target Adapters

iSYSTEM offers various adapter solutions for this POD. Please refer to the adapter documentation for more details.



T_QFP112 – Dimensions