

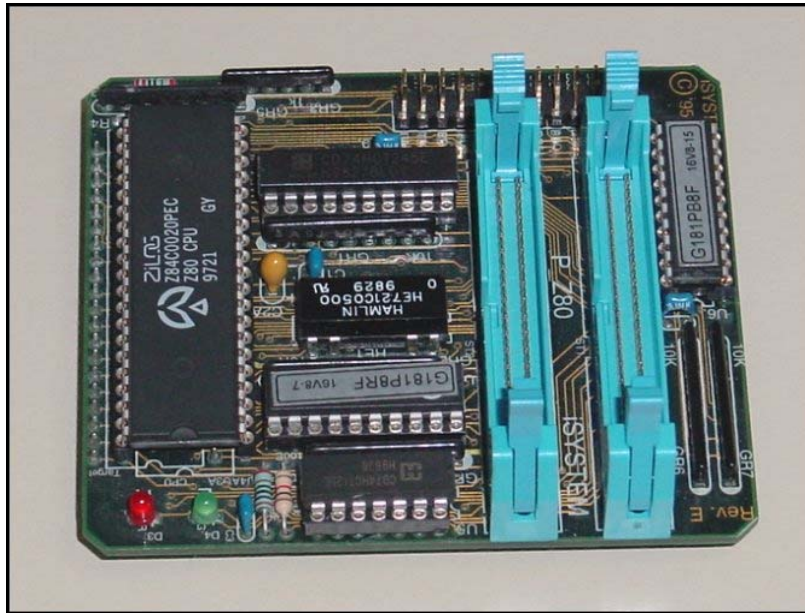
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## POD Hardware Reference

### Zilog Z80 POD rev. E

|               |            |
|---------------|------------|
| Ordering code | IC81010-20 |
|---------------|------------|



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## POD Hardware Reference

### In-Circuit Emulation PODs

The following elements of interest are located on all In-Circuit emulation PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED (D3) - lit when CPU is running
- green LED (D4) - lit when Emulator is ready for emulation
- a connector, mostly marked ST3 - contains signal lines, some of which are hardware configuration lines (such as bank select signals), others you can use for signal generation (pattern generator outputs).

Here are some common signals found on the signal connector, commonly marked as ST3:

- GND        Ground
- BPE        External breakpoint input. Active high.
- RESO/RO    Reset output. Connect to target to reset peripherals.
- TRES/TR    Target reset input.
- AUXn        AUX signal inputs (same as inputs on Emulator/trace)

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Note: On PODs that support synchronization between two or more Emulators (currently only the HC(S)12 Family, see the Synchronization section in the Hardware User's Guide for more information) AUX0 and AUX1 are cut short with Run/Stop synchronization line, and AUX2, AUX3 with RESET synchronization line. You should use these pins to connect to other PODs or target CPUs.

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- PAT0-2     Pattern generator output on 16-bit POD
- OC4-6     Pattern generator output on 8-bit POD

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Note: The signal connector can also have other markings, like P1, U1, etc. Please refer to the POD-specific documentation for the signal connector name and signals present.

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For every POD the following information is given:

- Ordering code. If there are different speed versions of a POD the ordering code is modified by appending the speed in MHz (IC81020-16 for the 16 MHz 8031 POD)
- information on available speed versions and required Emulator access time
- POD size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

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Note: The In-Circuit Emulator can emulate a processor or a microcontroller. Beside the CPU, additional logic is integrated on the POD. The amount of additional logic depends on the emulated CPU and the type of emulation. A buffer on a data bus is always used (minimal logic) and when rebuilding ports on the POD, maximum logic is used. As soon as a POD is inserted in the target instead of the CPU, electrical and timing characteristics are changed. Different electrical and timing characteristics of used elements on the POD and prolonged lines from the target to the CPU on the POD contribute to different POD characteristics. Consequently, signal cross-talks and reflections occur, capacitance changes, etc.

Beside that, pull-up and pull-down resistors are added to some signals. Pull-up/pull-down resistors are required to define the inactive state of signals like reset and interrupt inputs, while the POD is not connected to the target. Because of this, the POD can operate as standalone without the target.

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## Final Target Application Test

After the application is being more or less debugged and final application test is performed, it is recommended to remove all breakpoints and to close all debug windows (memory, SFR, watch...) to eliminate any possible influence of the emulator on the CPU execution. There were cases where the target application has been behaving differently with the target CPU inserted or the POD connected. If the debugger is configured to update some debug windows in real-time, the user may not be aware of that the CPU execution may be slightly disturbed. However, when the monitor access type is configured to update debug windows while the CPU is running, the CPU execution is disturbed significantly, depending on the necessary number of memory accesses to update opened debug windows.

There are cases when internal peripheral device requires read access of the particular register during the device configuration. The user has had SFR window opened and the necessary read access was actually performed by the debugger and not by the application as it would be correct. Therefore, the application was working fine with the emulator, but a standalone application didn't work correctly, as the peripheral device was not configured properly.

## For Better Understanding of the Hardware Reference: PIN 1 locations

There are several references to pin 1 in the manual and many jumper settings, CPU and pinout orientations rely on the correct location of pin 1. If sometimes the location of pin 1 is not clear, check the markings on the POD. If there are no markings, check the PCB board of the POD. Pin 1 is always marked on the PCB with a square pin (the other pins are round). The pin 1 location is also visible on the board in the hardware reference, if not any other way it can be identified by searching for the square pin.

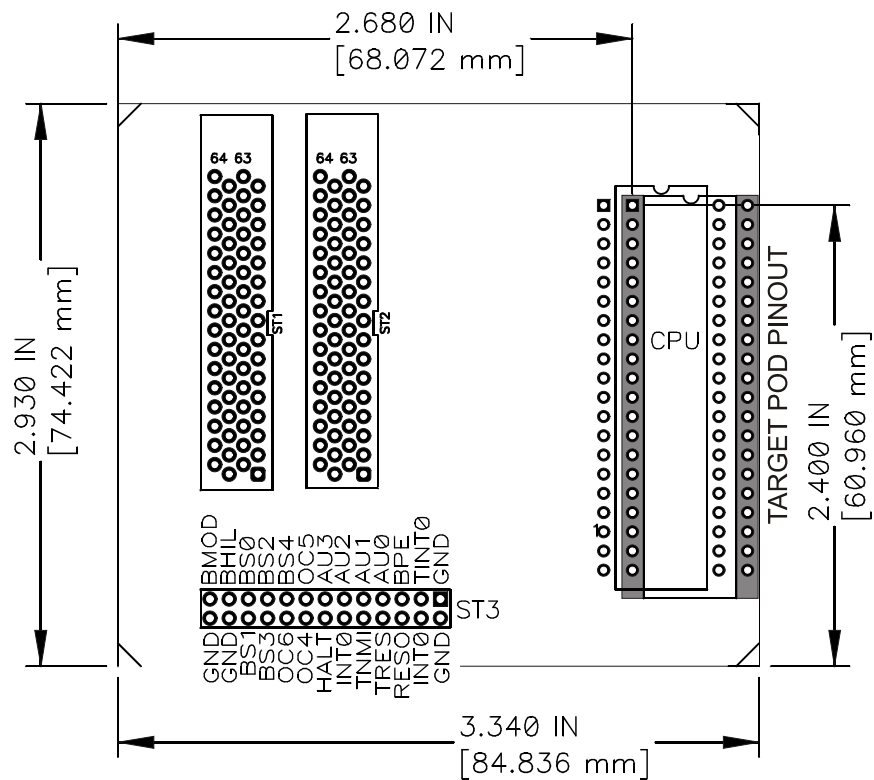
## POD Hardware Reference

### Zilog Z80 POD rev. E

|                            |                |           |           |
|----------------------------|----------------|-----------|-----------|
| <b>Ordering code</b>       | <b>IC81010</b> |           |           |
| <b>POD Speed (MHz)</b>     | <b>10</b>      | <b>12</b> | <b>12</b> |
| <b>Emulator Speed (ns)</b> | <b>150</b>     | <b>90</b> | <b>65</b> |
| <b>Bank switch support</b> | <b>YES</b>     |           |           |
| <b>Exchange CPU</b>        | <b>YES</b>     |           |           |

Please make sure you have read the technical notes on the Zilog Z80 Family in the Hardware User's Guide.

This POD is an 8-bit, 5-Volt only POD that can be used on iC181, iC1000 and the PowerEmulator unit.



| Emulated CPUs |
|---------------|
| Z80           |
| TMPZ84C013    |
| TMPZ84C015    |
| Z84013/C13    |
| Z84015/C15    |

Note: If you use an external clock on this POD, make sure that both timing and voltage level comply with Zilog's specification.

## The Signal Connector

A signal connector is present on this pod, marked as ST3.

| Description                                 | Signal | Pin | Pin | Signal | Description                                |
|---|--------|-----|-----|--------|--|
| Ground                                      | GND    | 26  | 25  | BMOD   | Bridge to GND when using banks             |
| Ground                                      | GND    | 24  | 23  | BHIL   | Not Used                                   |
| Bank Select Signal                          | BS1    | 22  | 21  | BS0    | Bank Select Signal                         |
| Bank Select Signal                          | BS3    | 20  | 19  | BS2    | Bank Select Signal                         |
| Pattern Generator Output                    | OC6    | 18  | 17  | BS4    | Not Used                                   |
| Pattern Generator Output                    | OC4    | 16  | 15  | OC5    | Pattern Generator Output                   |
| CPU signal for monitoring                   | HALT   | 14  | 13  | AU3    | AUX Input                                  |
| CPU signal for monitoring                   | INT0   | 12  | 11  | AU2    | AUX Input                                  |
| CPU signal for monitoring                   | TNMI   | 10  | 9   | AU1    | AUX Input                                  |
| Target Reset                                | TRES   | 8   | 7   | AU0    | AUX Input                                  |
| Reset Output                                | ROUT   | 6   | 5   | BPEXT  | External Breakpoint                        |
| Bridge with TINT to enable target interrupt | INT0   | 4   | 3   | TINT0  | Bridge with INT to enable target interrupt |
| Ground                                      | GND    | 2   | 1   | GND    | Ground                                     |

*ST3 Connector signals*

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Note: The BMOD signal must always be bridged to GND when banks are used.

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## Target POD Pinout

The target POD pinout is the standard DIP40.

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