

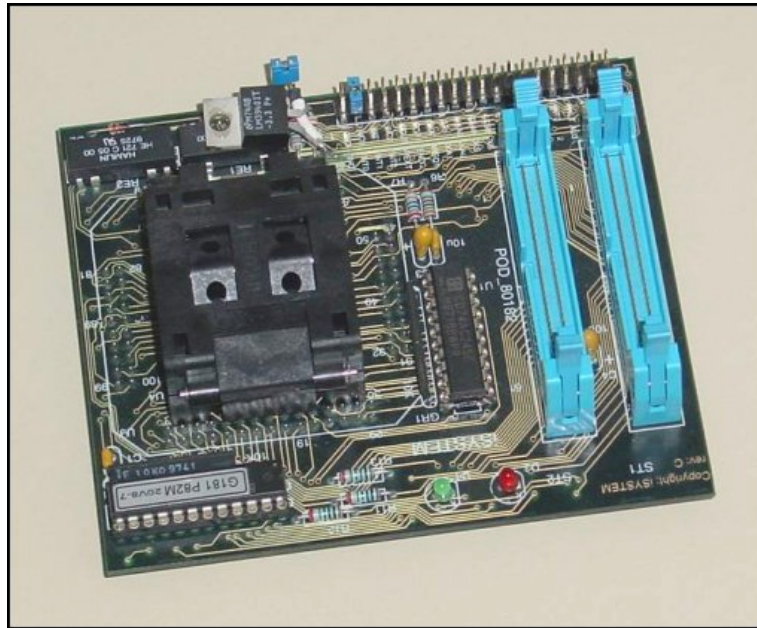
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## POD Hardware Reference

### Zilog Z80182 POD rev. A, B, C

<b>Ordering code</b>	<b>IC81015</b>
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## POD Hardware Reference

### In-Circuit Emulation PODs

The following elements of interest are located on all In-Circuit emulation PODs:

- emulation CPU - acts on behalf of target's CPU. On some PODs you must use the same CPU on the POD as it is used on the target (see your POD reference page). In such cases, remove the CPU from the POD and insert the CPU that you use in the target system, in its place.
- red LED (D3) - lit when CPU is running
- green LED (D4) - lit when Emulator is ready for emulation
- a connector, mostly marked ST3 - contains signal lines, some of which are hardware configuration lines (such as bank select signals), others you can use for signal generation (pattern generator outputs).

Here are some common signals found on the signal connector, commonly marked as ST3:

- GND        Ground
- BPE        External breakpoint input. Active high.
- RESO/RO    Reset output. Connect to target to reset peripherals.
- TRES/TR    Target reset input.
- AUXn        AUX signal inputs (same as inputs on Emulator/trace)

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Note: On PODs that support synchronization between two or more Emulators (currently only the HC(S)12 Family, see the Synchronization section in the Hardware User's Guide for more information) AUX0 and AUX1 are cut short with Run/Stop synchronization line, and AUX2, AUX3 with RESET synchronization line. You should use these pins to connect to other PODs or target CPUs.

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- PAT0-2     Pattern generator output on 16-bit POD
- OC4-6     Pattern generator output on 8-bit POD

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Note: The signal connector can also have other markings, like P1, U1, etc. Please refer to the POD-specific documentation for the signal connector name and signals present.

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For every POD the following information is given:

- Ordering code. If there are different speed versions of a POD the ordering code is modified by appending the speed in MHz (IC81020-16 for the 16 MHz 8031 POD)
- information on available speed versions and required Emulator access time
- POD size and position of PIN1 on the target adapter relative to bottom left corner.

The memory range specifies the range of addresses that a POD can address. If this specification is omitted the default 1MB is assumed.

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Note: The In-Circuit Emulator can emulate a processor or a micro-controller. Beside the CPU, additional logic is integrated on the POD. The amount of additional logic depends on the emulated CPU and the type of emulation. A buffer on a data bus is always used (minimal logic) and when rebuilding ports on the POD, maximum logic is used. As soon as a POD is inserted in the target instead of the CPU, electrical and timing characteristics are changed. Different electrical and timing characteristics of used elements on the POD and prolonged lines from the target to the CPU on the POD contribute to different POD characteristics. Consequently, signal cross-talks and reflections occur, capacitance changes, etc.

Beside that, pull-up and pull-down resistors are added to some signals. Pull-up/pull-down resistors are required to define the inactive state of signals like reset and interrupt inputs, while the POD is not connected to the target. Because of this, the POD can operate as standalone without the target.

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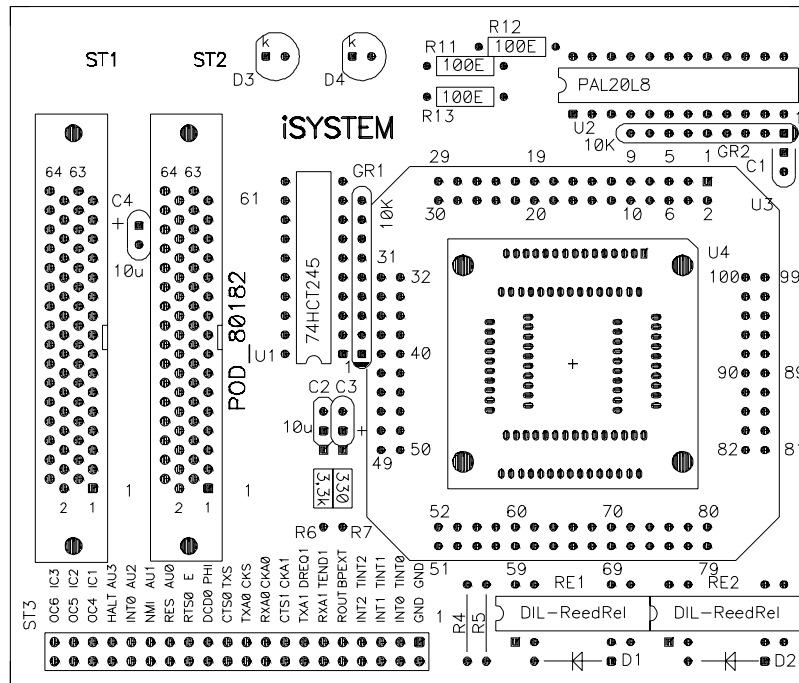
# POD Hardware Reference

## Zilog Z80182 POD rev. A, B, C

<b>Ordering code</b>	<b>IC81015-20</b>	
<b>POD Speed (MHz)</b>	<b>16</b>	<b>20</b>
<b>Emulator Speed (ns)</b>	<b>90</b>	<b>65</b>
<b>Bank switch support</b>	<b>MMU</b>	
<b>Dimensions (mm)</b>	<b>105x90</b>	
<b>Pin 1 position (mm)</b>	<b>92x67</b>	

This POD is an 8-bit, 5-Volt only POD that can be used on iC181, iC1000 and the PowerEmulator unit.

MMU bank switching is supported on this POD.



Top POD View

<b>Emulated CPU</b>
<b>Z80182</b>

Note that the input clock is normally internally divided by two. Thus if you run a 32MHz Z180, all operations are performed at 16MHz.

This POD supports the usage of a clip-over adapter.

## The Signal Connector

A signal connector is present on this pod, marked as ST3.

Description	Signal	Pin	Pin	Signal	Description
Pattern Generator Output	OC6	40	39	n.c.	not connected
Pattern Generator Output	OC5	38	37	n.c.	not connected
Pattern Generator Output	OC4	36	35	n.c.	not connected
CPU signal for monitoring	HALT	34	33	AU3	AUX Input
CPU signal for monitoring	INT0	32	31	AU2	AUX Input
CPU signal for monitoring	NMI	30	29	AU1	AUX Input
CPU signal for monitoring	RES	28	27	AU0	AUX Input
CPU signal for monitoring	RTS0	26	25	E	CPU signal for monitoring
CPU signal for monitoring	DCD0	24	23	PHI	CPU signal for monitoring
CPU signal for monitoring	CTS0	22	21	TXS	CPU signal for monitoring
CPU signal for monitoring	TXA0	20	19	CKS	CPU signal for monitoring
CPU signal for monitoring	RXA0	18	17	CKA0	CPU signal for monitoring
CPU signal for monitoring	CTS1	16	15	CKA1	CPU signal for monitoring
CPU signal for monitoring	TXA1	14	13	DREQ1	CPU signal for monitoring
CPU signal for monitoring	RXA1	12	11	TEND1	CPU signal for monitoring
Reset Output	ROUT	10	9	BPEXT	External Breakpoint
Bridge with TINT to enable target interrupt	INT2	8	7	TINT2	Bridge with INT to enable target interrupt
Bridge with TINT to enable target interrupt	INT1	6	5	TINT1	Bridge with INT to enable target interrupt
Bridge with TINT to enable target interrupt	INT0	4	3	TINT0	Bridge with INT to enable target interrupt
Ground	GND	2	1	GND	Ground

*ST3 Connector signals*

## Target POD Pinout

The target POD pinout is T\_QFP100.

29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

31	32
33	34
35	36
37	38
39	40
41	42
43	44
45	46
47	48
49	50

100	99
98	97
96	95
94	93
92	91
90	89
88	87
86	85
84	83
82	81

52	54	56	58	60	62	64	66	68	70	72	74	76	78	80
51	53	55	57	59	61	63	65	67	69	71	73	75	77	79

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