iTRACE Probe 2 MPC55xx/MPC56xx

Ordering code iTRACE Probe 2 MPC55xx/MPC56xx	IC30656

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Solutions for Embedded Systems Development

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Ordering code	IC30656
Dimensions (WxLxH, mm)	30x109x27

iSYSTEM is constantly adding support for new devices, therefore the list of emulated CPUs can change rapidly. For the latest list of emulated devices, please contact your local sales representative and/or check at www.isystem.com.

The iTRACE Probe 2 is used to connect the development system to the Freescale MPC5xxx or ST SPC56 based target. iTRACE Probe 2 is connected to the iTRACE GT unit, which then connects to iC3000 HS/GT unit.

Typically iTRACE GT unit comes assembled with a single flex cable marked with #1 designation. iTRACE Probe 2 MPC55xx/MPC56xx connects to #1 flex cable regardless of the number of flex cables attached to the iTRACE GT unit.

iTRACE Probe 2 features new technology, which allows automatic adjustment of a voltage threshold and phase at the input stage when the target signals are captured. iTRACE Probe 2 cannot be used with iTRACE PRO unit.

Jumper J2 (EVTIN)

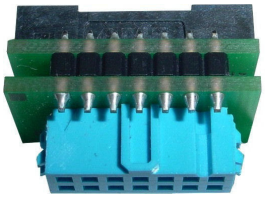
Under some circumstances it can happen that the debugger cannot find any absolute program counter message in the analyzed trace block. Consequentially, trace reconstruction fails and errors or nothing gets displayed in the trace window. To avoid such situations, the debugger can feed periodic signal to the EVTIN CPU pin connecting to the on-chip Nexus engine, which then periodically generates and broadcasts program counter synchronization messages.

In order to use this feature, jumper J2 must be bridged and the 'Force periodic Nexus SYNC' option in the 'Hardware/emulation Options/CPU Setup/Nexus' tab must be checked.

Note that the EVTI (Nexus Event In) CPU pin may be shared with other CPU functionalities. For instance, on MPC5516 the same pin can operate as GPIO, EBI read/write or EVTI. Whenever the CPU pin is configured and used for EVTI alternate operation, J2 must not be populated in order to prevent electrical conflicts..

Note: In general there is no need to use 'Force periodic Nexus SYNC' functionality unless a specific application code is traced, which does not generate messages containing absolute program counter information. As long as the user has no problems with the trace use, keep jumper 2 disconnected.

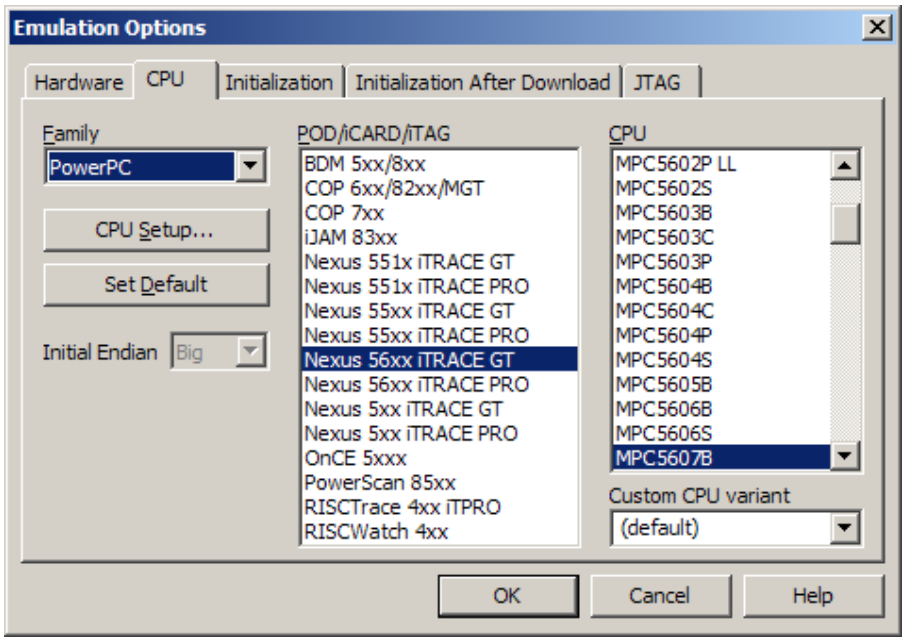
An adapter can be ordered separately under IAMIC38MPCPIN14 ordering code, which allows connecting the iTRACE Probe 2 to the 14-pin 2.54mm JTAG target debug connector, which does not feature Nexus interface.



When emulating MPC551x devices, 'Nexus 551x iTRACE GT' must be selected in the 'Hardware/Emulation Options' dialog (depending on the development system used) and then the target CPU.

When emulating MPC55xx devices, 'Nexus 55xx iTRACE GT' must be selected in the 'Hardware/Emulation Options' dialog and then the target CPU.

When emulating MPC56xx devices, 'Nexus 56xx iTRACE GT' must be selected in the 'Hardware/Emulation Options' dialog and then the target CPU.



Emulation Notes

The probe must not be inserted into the target if the target is turned on or damage to the Probe or iTRACE PRO/GT Interface Card can occur.

It is advised to first turn on the Emulator and then the target.

When external bus interface is used on the target CPU (MPC551x), no trace trigger can be used because a Nexus signal, reporting the trigger event, is not available when belonging CPU pins are configured for external bus interface operation. The user must properly configure the 'Nexus / EBI operation' setting in winIDEA 'CPU Setup' dialog according to the CPU usage. Refer to OCD PowerPC 55xx Technical Notes document for more details on all the settings.

Trace Line Calibration

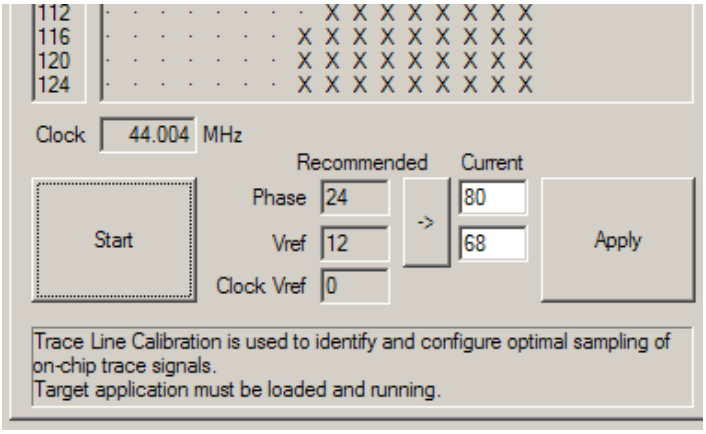
Majority of the modern embedded microcontrollers providing trace functionality, implements a so called message based trace port, where an individual trace message is broadcasted off the microcontroller through a relatively narrow physical trace port in multiple CPU cycles, at frequencies, which can be well over 100 MHz. Typically, the trace port is combined from trace data lines and a trace clock line, which is used to sample trace data lines on rising, falling or both edges (depending on the individual implementation).

At lower frequencies and good signal integrity we can consider the clock and data lines as pure digital signals, which are correctly phase aligned. As such, the external trace tool can capture them accurately without any problems.

Nowadays, capturing of the valid trace data becomes more and more challenging due to the various signal integrity issues (noise, skew, crosstalk, reflections, ground bounce…), which are introduced either due to the high frequency trace clock & data, due to the bad target PCB design or a combination of both. iTRACE Probe 2 has the ability to compensate for these issues via Trace Line Calibration functionality, which allows shifting threshold voltage and clock phase at the capture time of the trace data. When Trace Line Calibration is performed, it auto scans over these two dimensions and searches for valid and invalid settings and finds an optimum data eye.

Example

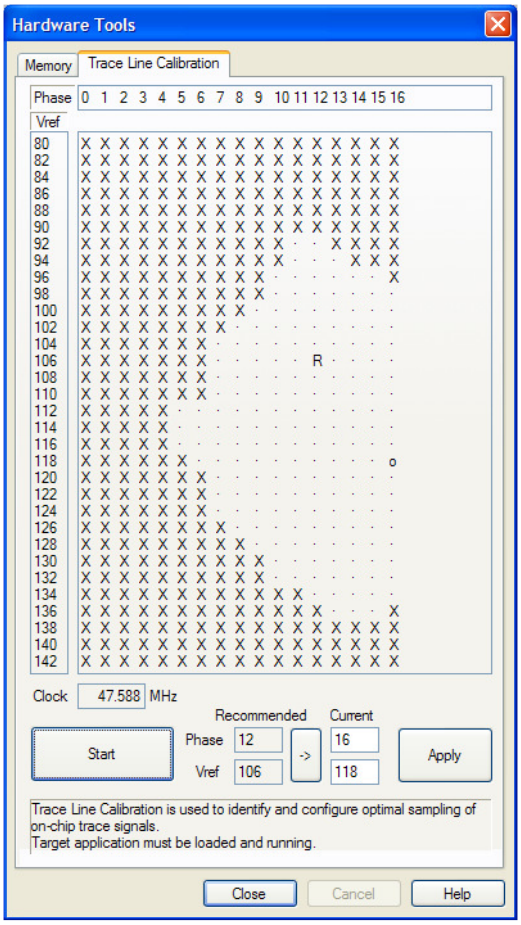
Let's assume we have a Cortex-M3 based NXP LPC1768 microcontroller running at 95 MHz. At this frequency, some of the signal integrity issues will show up for sure. After the debug download, the application should be run. Next, the "Start" button in the "Hardware/Tools/ Trace Line Calibration" should be pressed, which starts the auto-scan. After a couple of seconds, the result of the scan is collected and recommended "Vref" and "Phase" values are provided. Typically, the user just needs to press the "->" button to use the recommended values (or, if desired, enter them manually) and finally use the Apply button.



Configuration part of the Trace Line Calibration dialog

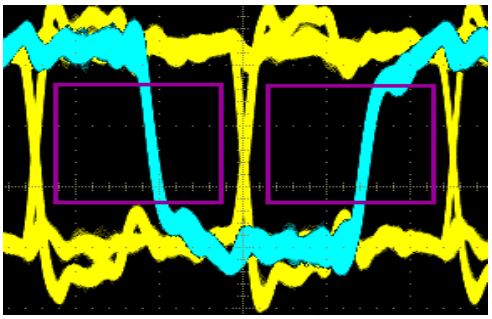
Newly applied values are stored upon Save Workspace and also used on the next debug download.

The following picture shows the result of the Trace Line Calibration and the corresponding timing view of signals on the trace port.



Trace Line Calibration window – scan has been performed and applied.

X	invalid area
.	valid area
R	recommended
o	currently used



Good signal integrity at lower frequency with large "Data eyes"

Higher frequency: Valid "Data eyes" shown on upper data signal and how the clock (lower) must be delayed.

Trace Port PCB Design Guidelines

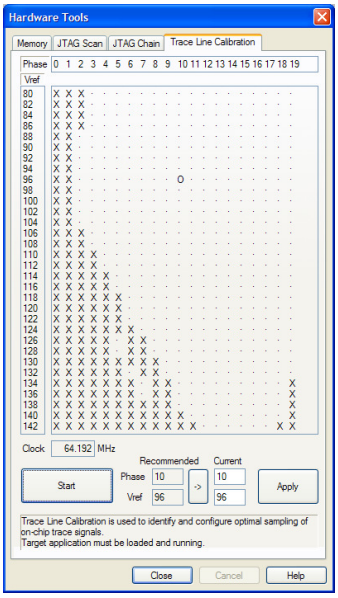
This section contains some guidelines, which should be considered during the target PCB design to ensure the correct operation of the trace port (ETM, Nexus,…) and the external trace tool (iC5000, iTRACE GT). Note that the quality and timing of the trace port signals to the external trace tool are critical for correct and reliable trace operation.

- All trace port lines on the PCB should be as short as possible (max ~2,5 cm),
- Traces should run on the same layer, or layers with the same impedance.
- Preferred layer impedance is 50 Ohm.
- Mictor ground pins should be connected directly to PCB's GND plane.
- Trace clock should be serially terminated by 47 Ohm resistor as close as possible to the driver. The value of the resistor may be changed depending on driver characteristics.

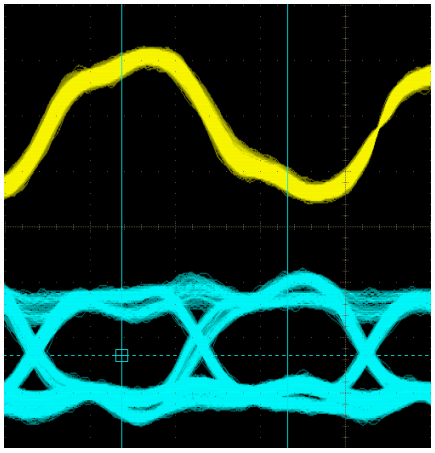
- Trace clock should be clean of crosstalk – if possible with double distance to closest nets.
- Trace clock should have only point-to-point connection – any stubs should be avoided.
- It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they should be as short as possible, when longer are required, there should be a possibility to optionally disconnect them (e.g. by jumpers).
- Trace port data bus inner crosstalk is not so important, but it is critical to isolate the whole bus from other signals (including from the trace port clock).

The following examples show, how the length of the trace lines is reflected in signal integrity and consequently in functionality. One of typical evaluation boards was used, where the CPU is located on the upper piggyback board, which fits to the lower, larger measurement board.

Trace lines with short stubs

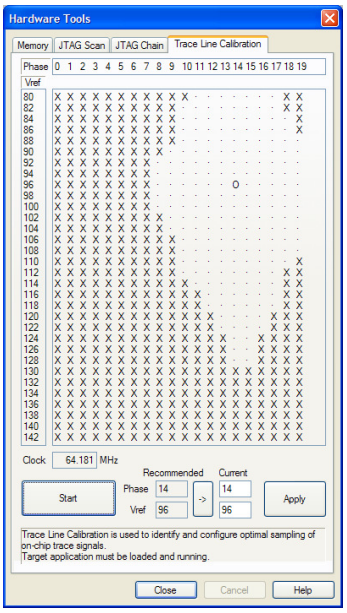


Trace Line Calibration result

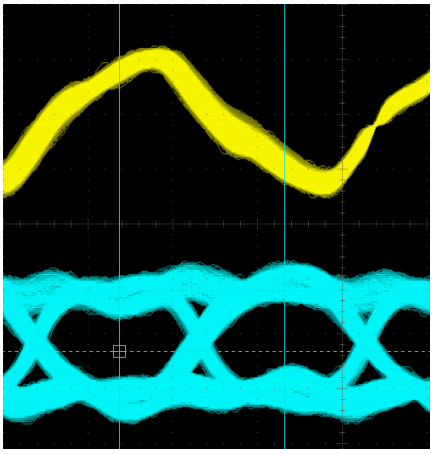


Measured by oscilloscope

Trace lines with longer stubs (over connector to other board)



Trace Line Calibration result



Measured by oscilloscope

Target Debug Connector Pinout

The iTRACE Probe 2 MPC55xx/MPC56xx features a 38-pin Mictor connector (Tyco Electronics 5767055-1). A target should feature a matching part (for example Tyco Electronics 5767081-1 in SMT technology).

Signal	Pin	Pin	Signal
MDO12	1	2	MDO13
MDO14	3	4	MDO15
MDO9	5	6	CLKOUT
BOOTCFG	7	8	MDO8
RSTIN	9	10	EVTIN
TDO	11	12	VTREF
MDO10	13	14	RDY
TCK	15	16	MDO7
TMS	17	18	MDO6
TDI	19	20	MDO5
NTRST	21	22	MDO4
MDO11	23	24	MDO3
Not used	25	26	MDO2
Not used	27	28	MDO1
Not used	29	30	MDO0
Not used	31	32	EVTO
Not used	33	34	MCKO
Not used	35	36	MSEO1
Not used	37	38	MSEO0

PowerPC 55xx/56xx Nexus Mictor 38-pin target layout

Input, Output Signals

The input signals EVTO, MSEO0..1, MCKO and MDO0..15 have 1Mohm impedance. The voltage must be between 1.8 and 5V.

The output signals RSTIN, EVTI, NTRST are push-pull outputs, where the output voltage is equal to 3.3V or equal to VTRef, if VTRef is lower than 3.3V. If VTref is higher, then it is limited to 3.3V.

The VTRef is an input with the resistance of 1Kohm and is used only for reference. Its value can be between 1.8 and 5V.

The threshold for inputs is ½ VRef, if VRef is 3.3V or lower. If VRef is higher than 3.3V, the threshold is ½ of 3.3V. The minimal VRef is 1.8V.

Operating temperature range

All iSYSTEM devices, unless explicitly otherwise noted, are specified to operate at room temperatures (specifically, between 10°C/50°F and 40°C/105°F).