V 20.1

02.1.1 INTRODUCTION TO ARM CORTEX-M TRACE

Introduction to ARM Cortex-M Trace

Contents

01 Cortex-M CoreSight Debug and Trace Architecture

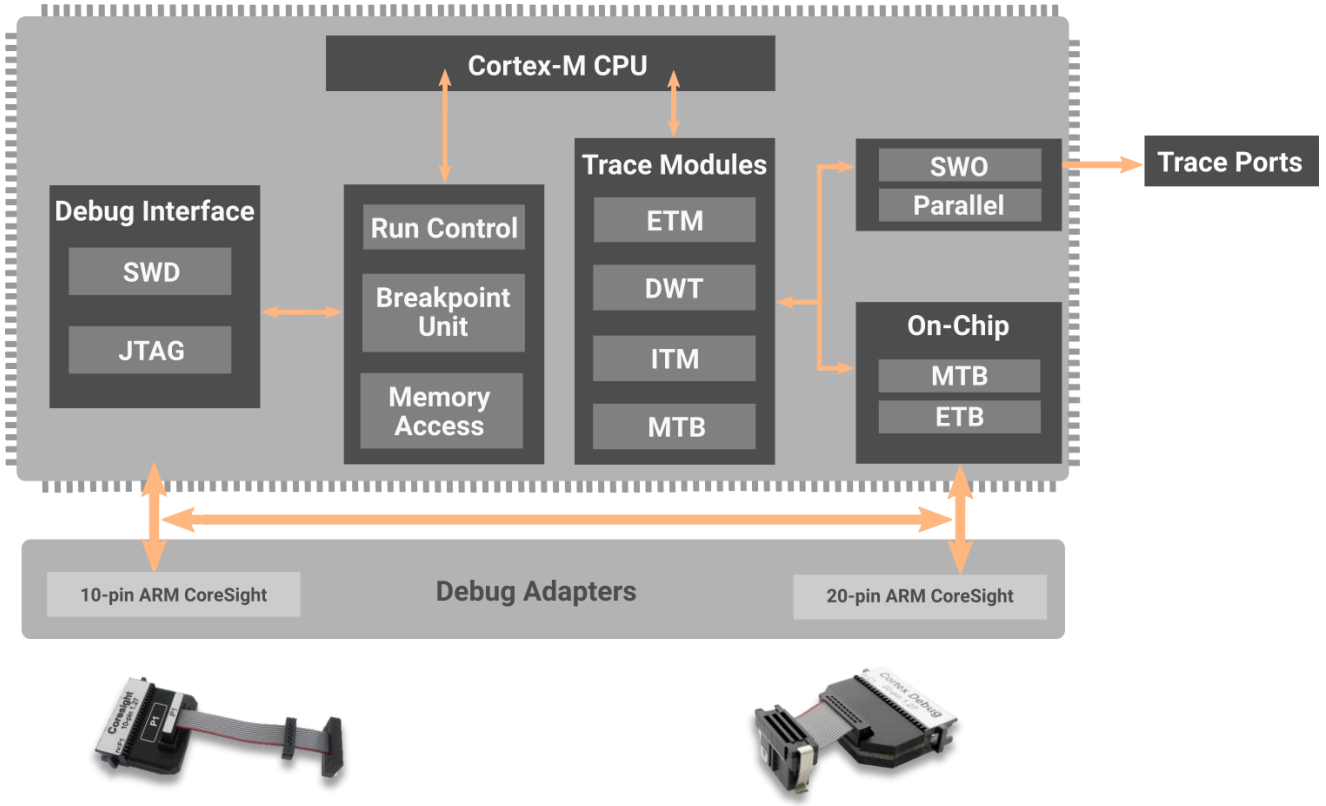
ARM CoreSight architecture allows debugging and tracing software which runs on microcontroller or SoC. Trace data is typically captured off-chip but it can be also stored on-chip:

OFF-CHIP – Trace data is first captured and then streamed via the BlueBox to the PC:

- **Parallel** – Streams trace data via dedicated parallel trace pins
- **SWO** (Single Wire Output) – Streams trace data via single trace pin

ON-CHIP – Trace data is recorded to the internal memory trace buffer and read through the debug interface: Buffer can be:

- ETB – Embedded Trace Buffer
- MTB – Micro Trace Buffer



02 Cortex-M0+ Trace Architecture

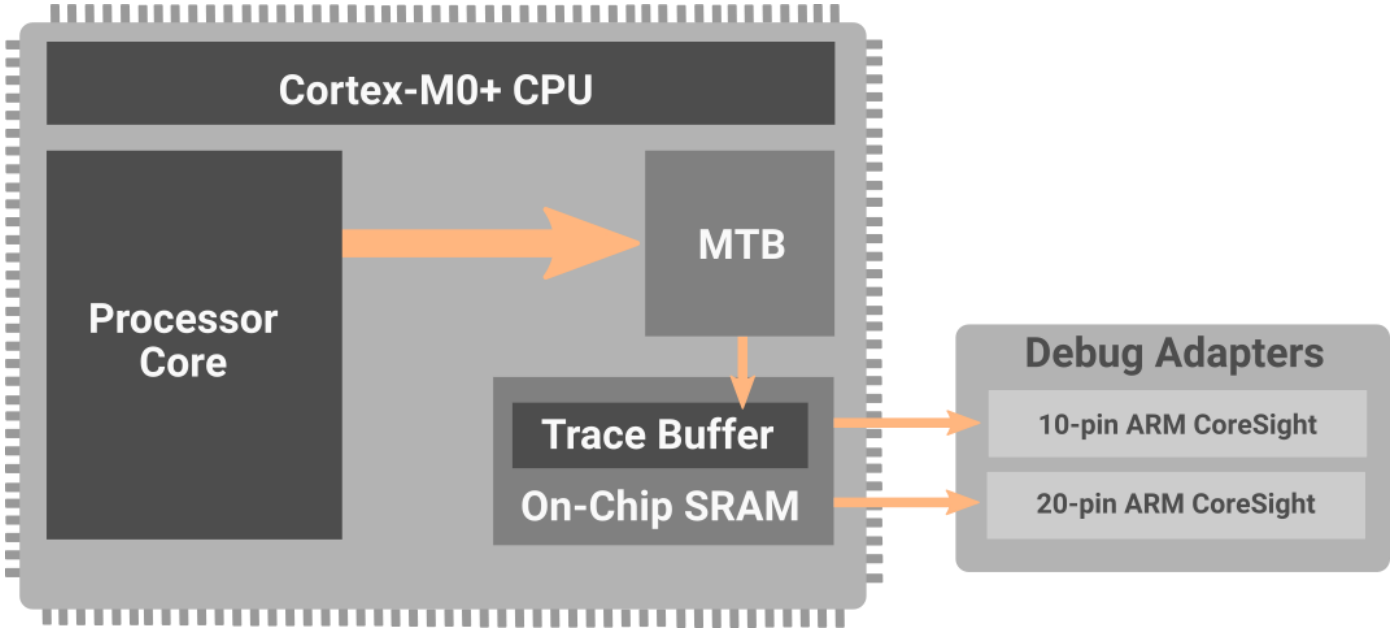
Micro Trace Buffer (MTB) trace component is available on some Cortex-M0+ microcontrollers and provides a simple program trace capability.

Trace data is saved to the trace buffer which is a dedicated area of the on-chip SRAM. The on-chip SRAM assigned to the MTB must not be used by the application while tracing.

After trace data is saved, the BlueBox reads it out and reconstructs the program flow.

Limitations:

- Small buffer, typically between 2kB and 8kB
- No time information
- No data trace



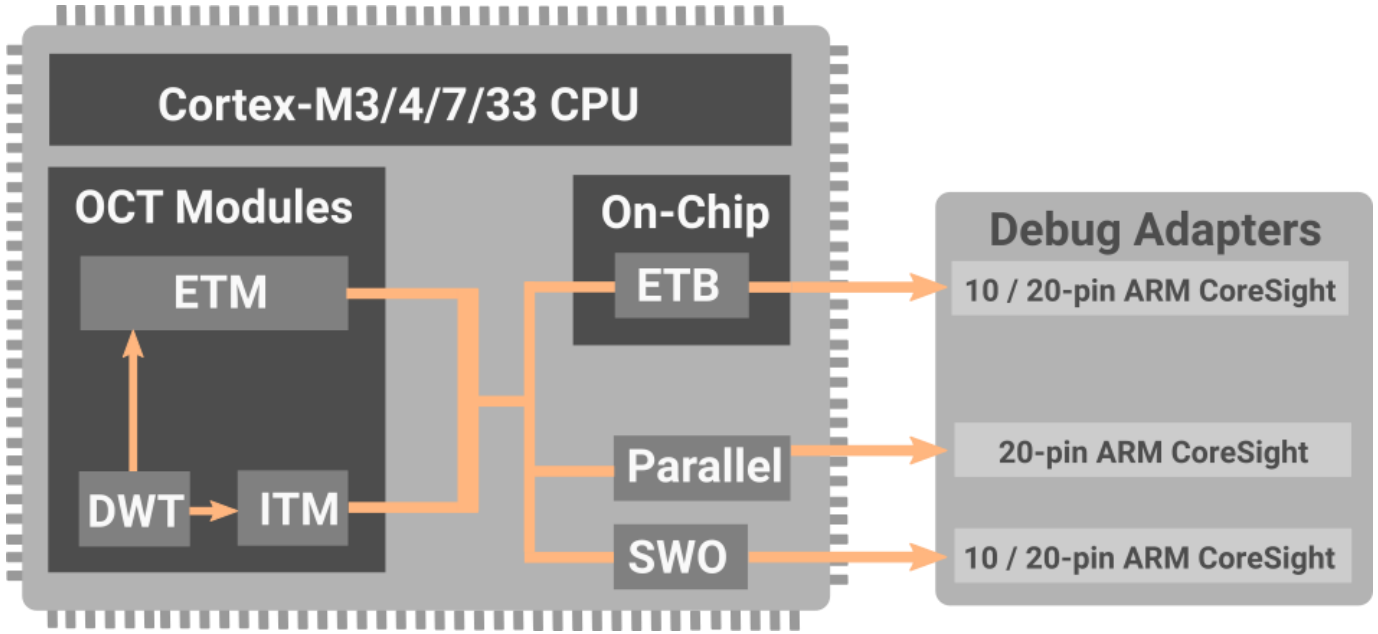
03 Cortex-M3/4/7/33 Trace Architecture

Cortex-M3/4/7/33 based CPUs typically contain one or more trace components:

- **ITM** (Instrumentation Trace Macrocell) provides software instrumented trace (printf() style), timestamps for the ITM and the DWT trace messages and integrates the DWT trace messages into the trace stream.
- **DWT** (Data Watchpoint & Trace Unit) features interrupt trace, data trace, PC sampler and ETM trigger. The DWT output is fed into the the ITM.
- **ETM** (Embedded Trace Macrocell) features program trace. ETM can act on events from the DWT.

Trace capture methods supported on Cortex-M3/4/7/33 are:

- On-Chip: ETB
- Off-Chip: Parallel, SWO



04 Cortex-M Trace Components Overview

Cortex-M series of cores can feature different trace components.

The table shows available trace components across different Cortex-M architectures.

Core	Cortex-M0/1	Cortex-M0+	Cortex-M23	Cortex-M3/4/7	Cortex-M33
Architecture	ARMv6-M	ARMv6-M	ARMv8-M	ARMv7-M	ARMv8-M
MTB		✔	✔		
DWT	✔	✔	✔	✔	✔
ETM			✔	✔	✔
ITM				✔	✔

**Not all cores support all trace modules. Refer to microcontroller documentation.*

05 Trace Capture Methods Overview

iSYSTEM tools support all Cortex-M trace capture methods.

The table offers a quick overview of the available trace capture methods along with the target connection requirements, their advantages and disadvantages.

Trace Capture method	Target connection requirements	Advantages	Disadvantages
PARALLEL	SWD or JTAG Debug Protocol 20-pin ARM CoreSight Debug Adapter	Exact time information Available with JTAG and SWD High bandwidth	Requires trace pins
SWO	SWD Debug Protocol 10 / 20-pin ARM CoreSight Debug Adapters	Available with all Debug Adapters ITM and DWT	Available only with SWD Low bandwidth
MTB	All combinations possible	Power efficiency Low cost trace solution No trace pins needed	Small trace buffer No time information Available only on Cortex-M0+ Program trace only, no data
ETB	All combinations possible	No trace pins needed	Small trace buffer No time information

Further Reading

For more information refer to our online resources:

Hardware Solutions:

- On-Chip Analyzer BlueBox iC5700
- Active Probes
- Debug Adapters

winIDEA Online Help:

- winIDEA Analyzer
- ARM Cortex Analyzer

Knowledge Base