V 20.2

02.2.2 AURIX winIDEA CONFIGURATION

AURIX winIDEA Configuration

Contents

01 CPU Options

Specific CPU Options need to be configured prior to using the Analyzer.

First you need to determine:
- Does the CPU support trace?
- Are CPU trace pins available on the Target?
- Does the Debug Adapter match the Target debug connector?
- Is the Trace activation key programmed in the BlueBox?

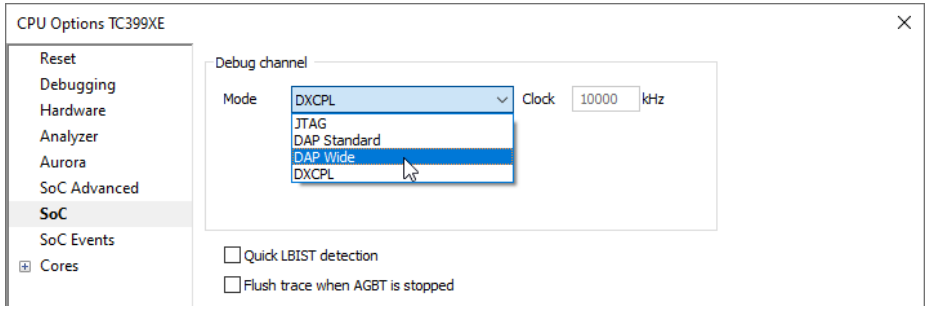
winIDEA Analyzer Configuration is mainly done in *Hardware menu / CPU Options* dialog in:
- SoC tab
- Analyzer tab
- Aurora tab

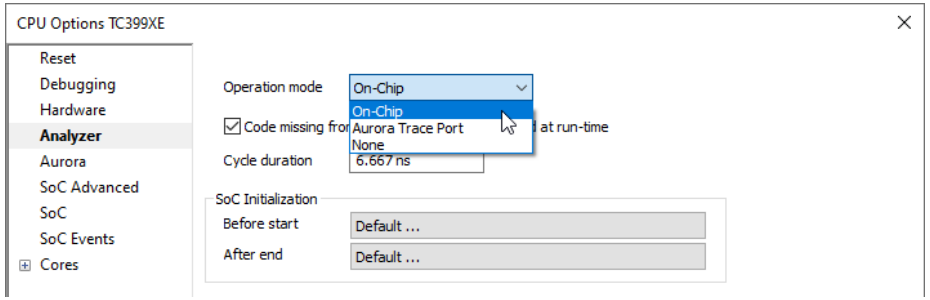
This unit describes settings in the CPU Options dialog.

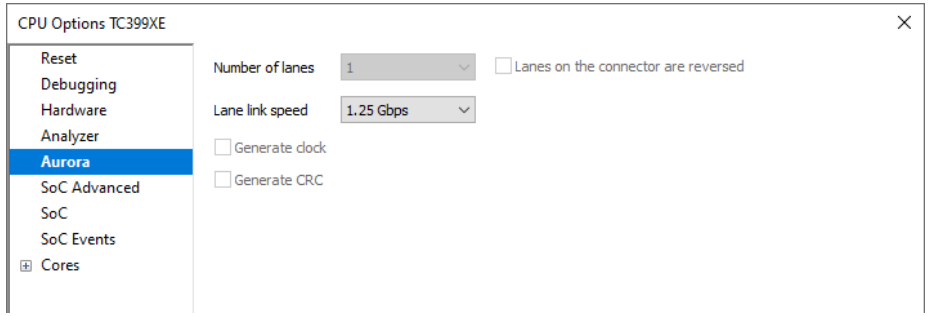
General Analyzer Configurations dialog settings are explained in detail in Analyzer – Trace or Analyzer – Profiler unit.

__TIP:__ Naming system can indicate whether an AURIX device supports trace, e.g.:
- ***E, F** (only TC2xx) – Emulation Device (TC375__TE__, TC277__TE__, TC299__TF__)*
- ***P, "-"** (TC2xx) – Production Device (TC377T__P__, TC275T__P__)*

For more information refer to TriCore Naming Convention.







02 Debug channel Mode – DAP / JTAG

A debug session needs to be established prior to using the Analyzer. First step is to select correct Debug channel Mode:

1. Select **DAP Standard** or **DAP Wide** according to the Target debug connector layout in *Hardware menu / CPU Options / SoC tab*. Default DAP Clock setting should work in most cases.

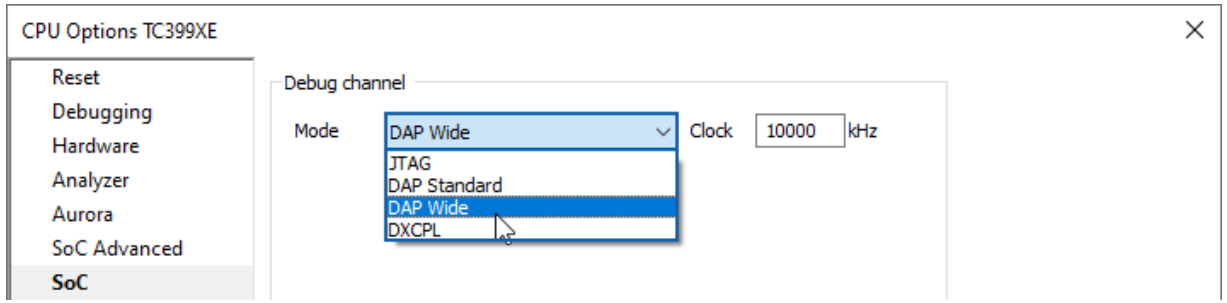
For better performance:
Use DAP Wide if supported by the CPU and all necessary signals are connected to the target debug connector
- *Use the highest DAP Clock as possible*

JTAG interface is supported as well, however it is recommended to use DAP Debug interface since it's faster.

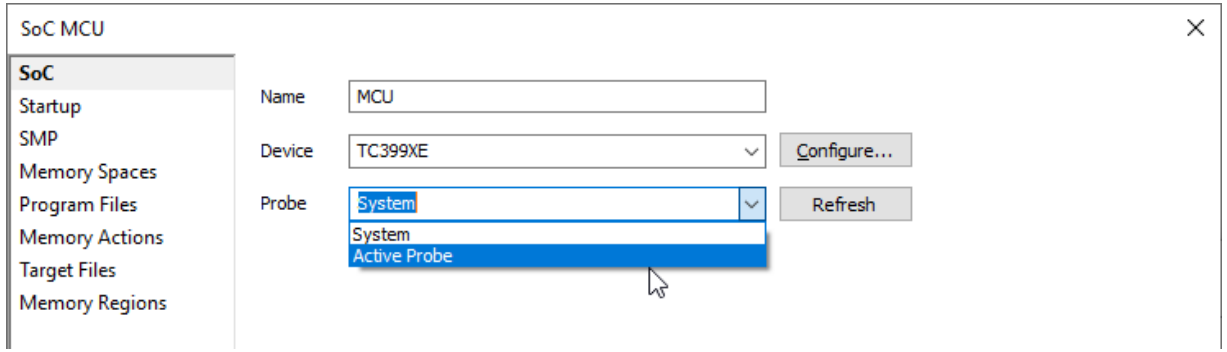
2. If you are using an Active Probe, make sure the correct Probe is selected in *Hardware menu / Emulation Options*
Refer to Knowledge Base when having issues with the Active Probe.

Read more about this setting in the Tutorial CPU Specific Architecture Settings – pages 9 - 12.

1



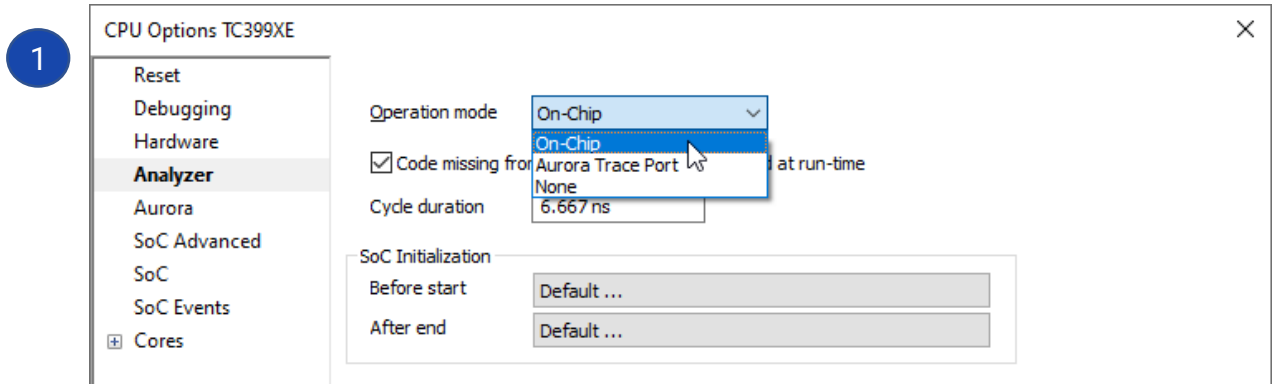
2



03 Operation mode

Open *Hardware menu / CPU Options / Analyzer tab* and select Operation mode according to the Debug connector on the Target.

1. Select **Operation mode:**
- On-Chip (default) or
- Aurora Trace Port – only when connected to the AGBT port (iC5700 & Infineon AGBT Active Probe or iC6000 – Refer to page 10 for details).



04 Clock configuration via the Aurix Plugin

1. Specify **Cycle duration** – the MCDS Clock cycle duration, which can be obtained via the **Aurix Plug-in.**

2. **Aurix Plug-in:** Open *View menu / <device>.Aurix* and click the **Refresh** button while the CPU is running.

The Plug-in will display the current MCDS Clock in Hz. For higher CPU Clock frequencies, the MCDS clock is typically half the CPU Clock.

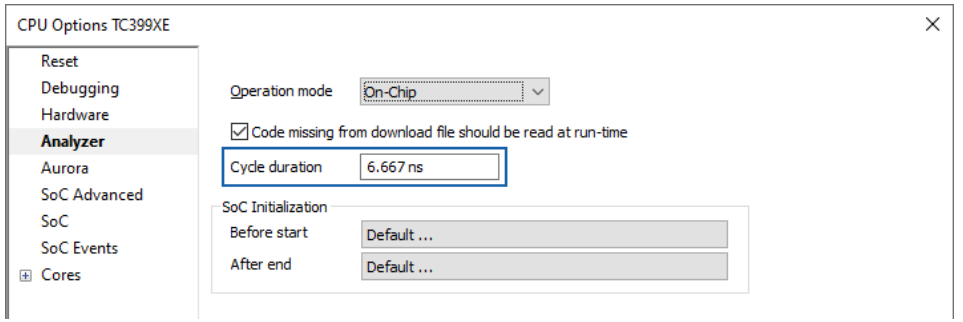
Example: *The MCDS Clock is running at 149967 kHz. Therefore the Cycle duration is 6.67 ns.*

$$Cycle\ duration\ (ns) = \frac{1}{MCDS\ Clock\ (MHz)} * 1000$$

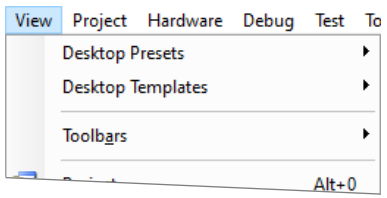
4. If you use following interfaces go to:
- DAPE Interface – page 7
- AURORA (AGBT) Interface – page 10

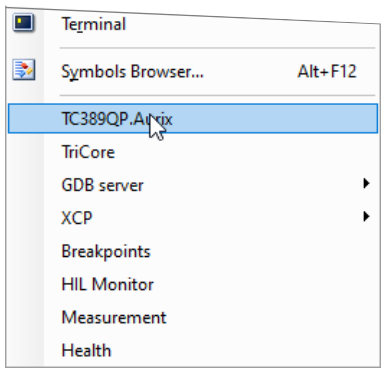
In winIDEA 9.17.153 and older versions, the information about MCDS Clock can be calculated in the TriCore Plug-in.

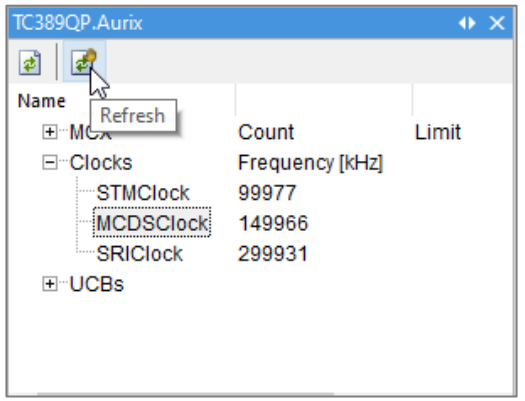
1



2







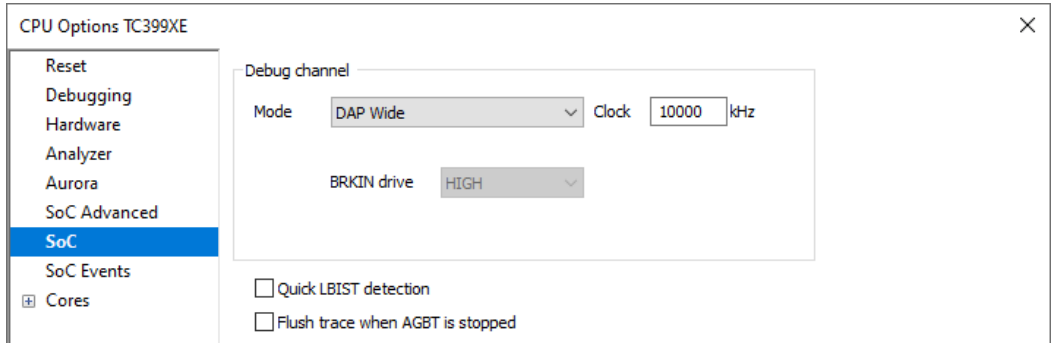
05 DAPE Interface

Configure DAPE settings if you are using iC5700, Infineon DAP/DAPE Active Probe and DAPE connection to the target.

1. Enable **DAPE** and select **DAP Standard** or **DAP Wide** (Default) Mode from the drop-down list.

Default DAPE Clock setting should work in most cases.

2



06 On-Chip Trace Buffer 1/2

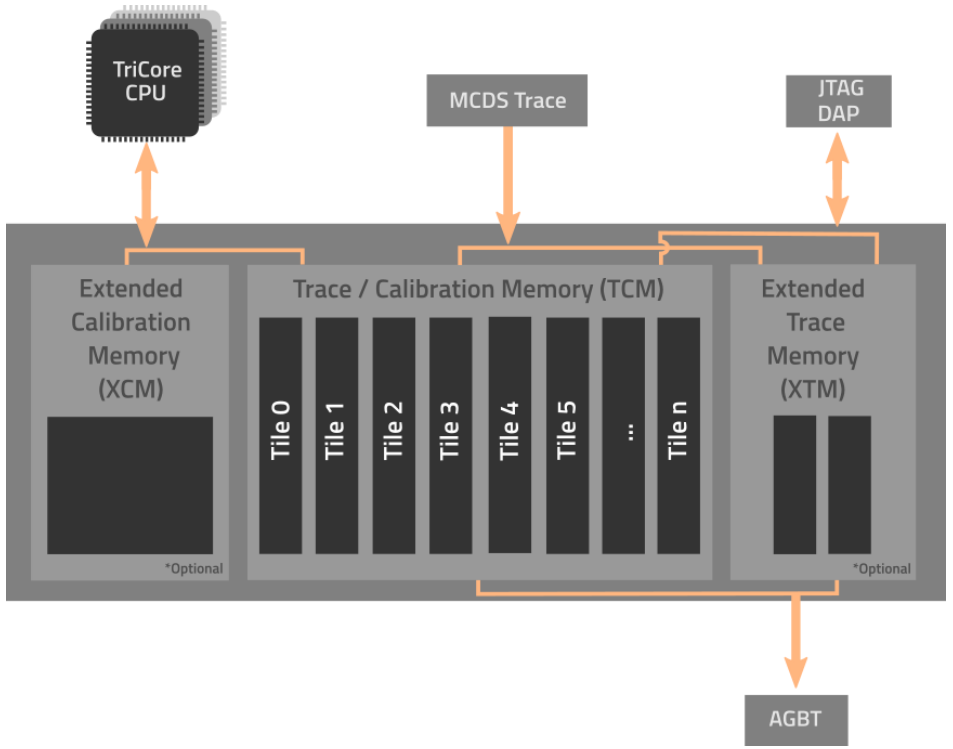
Trace is available only on dedicated Emulation Devices. Regular production devices don't provide Trace capability.

In this case Trace data is stored in the so-called Emulation Memory (EMEM).

The structure of the EMEM (for a TC2x emulation device) is depicted on the right.

By default Emulation Memory consists of a regular memory array (TCM – Trace Calibration Memory) built out of RAM Blocks (Tiles), which can be split in a Trace memory and a Calibration memory part.
Additionally certain Emulation Devices (ED) offer the optional memory XTM (Extended Trace Memory) for Trace. XTM can be also assigned to Calibration.

If the Emulation Device with AGBT has TCM or XTM assigned to Trace, TCM Tile0 respectively XTM Tile0 acts as AGBT Trace buffer.



Refer to the AURIX Trace Overview and Use-Cases Application Note page 11 for more information.

06 On-Chip Trace Buffer 2/2

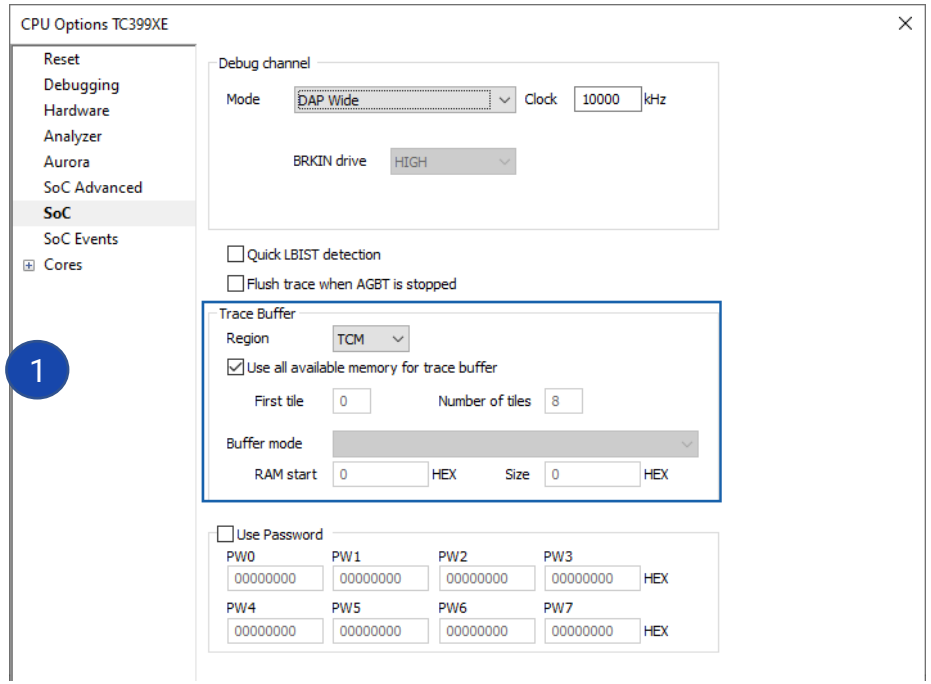
Trace Buffer is configured in *Hardware menu / CPU Options / SoC tab.*

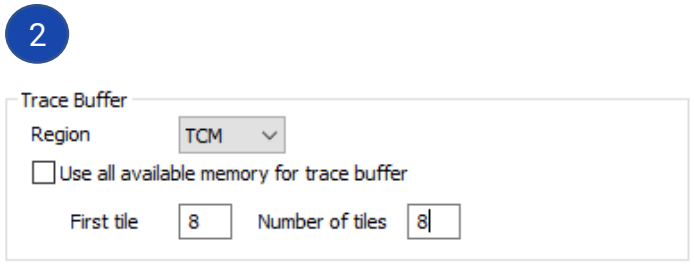
1. Default configuration **Use all available memory for trace buffer** option checked should work in most cases assuming that complete TCM memory is available for Trace.

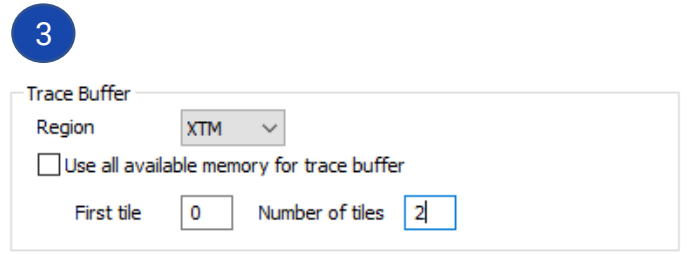
2. When limited amount of TCM memory respectively Tiles are available for Trace (the rest is used for Calibration), specify TCM Tiles reserved for Trace accordingly. Note that Trace buffer can consists of consecutive Tiles only. Define the **First tile** and define **Number of tiles** available for trace.

3. When whole TCM memory is used for Calibration and the Emulation Device provides optional XTM memory, which is available for Trace, specify XTM Tiles reserved for Trace accordingly.

Refer to in Analyzer – Trace or Analyzer – Profiler unit. to start using the Trace respectively the Profiler.







07 AGBT (Aurora) Interface

Configure this setting if you are using iC5700 & Infineon AGBT Active Probe or iC6000.

1. Select **Aurora Trace Port** Operation mode in *Hardware menu / CPU Options / Analyzer tab.*

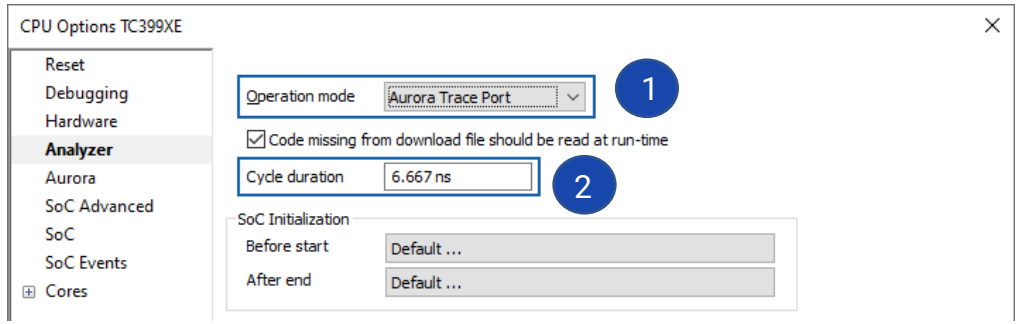
2. Specify **Cycle duration** via the Aurix Plug-in (page 6) and confirm by clicking OK.

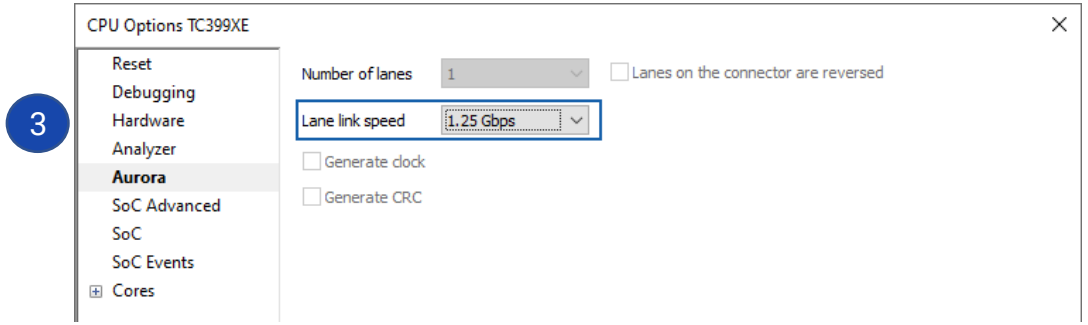
3. Open *Aurora tab* and select **Lane link speed** from the drop-down menu. If possible, select the higher bitrate to allow a maximum trace bandwidth.

By default the lowest link speed is set which ensures the most likely working trace operation. Note that this setting directly impacts on Aurora trace interface bandwidth. The higher the link speed, more trace information can be broadcasted over the interface.

Number of lanes – Most AURIX Devices support only 1 Aurora lane.

4. For **TC2xx:** Refer to in Analyzer – Trace or Analyzer – Profiler unit to start using the Trace respectively the Profiler.





Further Reading

For more information refer to our online resources:

- Hardware Solutions:
  - On-Chip Analyzer BlueBox iC5700
  - Active Probes
  - Debug Adapters
- winIDEA Online Help:
  - winIDEA Analyzer
  - Infineon TriCore Online Help
  - Plugins TriCore and Aurix
- iSYSTEM Infineon Microcontrollers overview
- Application Note – AURIX Trace Overview and Use-Cases
- Knowledge Base