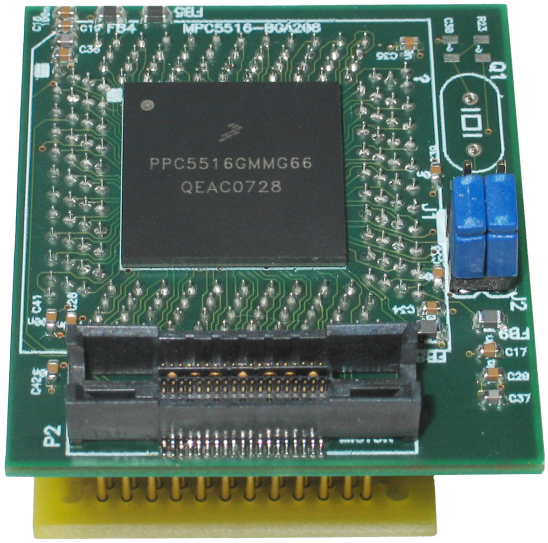
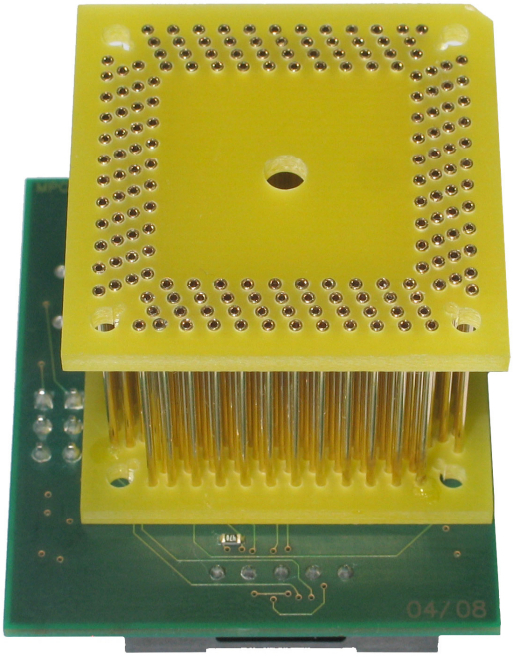
MPC5517 Nexus Emulation Board 208BGA – 176TQ

Ordering code	IA208BGA176TQ-5517





Target CPU package: T_QFP176

The original MPC5517 device has port F, on which alternate operations beside the default GPIO operation are possible. One of the possible operations is for it to be used as a Nexus port used for development. When a user connects an external development tool to the port F, this port is lost for the application.

This adapter is an alternative solution for the MPC5517 development. The Nexus Emulation Board is based on a MPC5517 device in the BGA208 package. The emulator connects to port F in the BGA208 device and then the ports J, H and E from the BGA208 device are connected to port F, replacing the lost Port F signals of the MPC5517 device. Consequently, the target application must be adjusted in order to use ports J, H and E instead of port F to which the external development tool connects.

Original connection	Replacement connection
PF0 – PF3	PJ0 – PJ3
PF4 – PF6	PE7 – PE9
PF7	PH12
PF8 – PF15	PF8 – PF15

This solution can only be used as long as the replaced port F pins are used as GPIO in the target application. Also, interrupts on GPIO can not be used on port F.

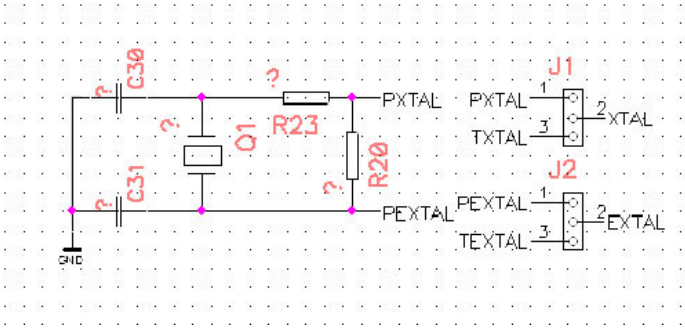
Target Pad ID	Emulation Pad ID	Original SIU_PCR Address (port F)	Emulated SIU_PCR Address (port J, E, H)	Original SIU_GPDO Address (port F)	Emulated SIU_GPDO Address (port J, E, H)	Original SIU_GPDI Address (port F)	Emulated SIU_GPDI Address (port J, E, H)
PF0	PJ0	FFFE80E0	FFFE8140	FFFE8650	FFFE8680	FFFE8850	FFFE8880
PF1	PJ1	FFFE80E2	FFFE8142	FFFE8651	FFFE8681	FFFE8851	FFFE8881
PF2	PJ2	FFFE80E4	FFFE8144	FFFE8652	FFFE8682	FFFE8852	FFFE8882
PF3	PJ3	FFFE80E6	FFFE8146	FFFE8653	FFFE8683	FFFE8853	FFFE8883
PF4	PE7	FFFE80E8	FFFE80CE	FFFE8654	FFFE8647	FFFE8854	FFFE8847
PF5	PE8	FFFE80EA	FFFE80D0	FFFE8655	FFFE8648	FFFE8855	FFFE8848
PF6	PE9	FFFE80EC	FFFE80D2	FFFE8656	FFFE8649	FFFE8856	FFFE8849
PF7	PH12	FFFE80EE	FFFE8138	FFFE8657	FFFE867C	FFFE8857	FFFE887C
PF8	PF8*	FFFE80F0	FFFE80F0	FFFE8658	FFFE8658	FFFE8858	FFFE8858
PF9	PF9*	FFFE80F2	FFFE80F2	FFFE8659	FFFE8659	FFFE8859	FFFE8859
PF10	PF10*	FFFE80F4	FFFE80F4	FFFE865A	FFFE865A	FFFE885A	FFFE885A
PF11	PF11*	FFFE80F6	FFFE80F6	FFFE865B	FFFE865B	FFFE885B	FFFE885B
PF12	PF12	FFFE80F8	FFFE80F8	FFFE865C	FFFE865C	FFFE885C	FFFE885C
PF13	PF13	FFFE80FA	FFFE80FA	FFFE865D	FFFE865D	FFFE885D	FFFE885D
PF14	PF14	FFFE80FC	FFFE80FC	FFFE865E	FFFE865E	FFFE885E	FFFE885E
PF15	PF15	FFFE80FE	FFFE80FE	FFFE865F	FFFE865F	FFFE885F	FFFE885F

The user can decide to use either a 4 or 8-bit Nexus port. This selection is done by setting the ‘Nexus MDO width’ in the ‘Hardware/Emulation Options/Debugging’ tab.

Both configurations have advantages and drawbacks. With an 8-bit Nexus configuration, the Nexus port has more bandwidth and is less prone to overflows when using trace. With a 4-bit Nexus configuration, pins PF8..15 are original port F ports. When an 8-bit Nexus port is used, PF8..11 can not be used for the application while PF12..15 are available.

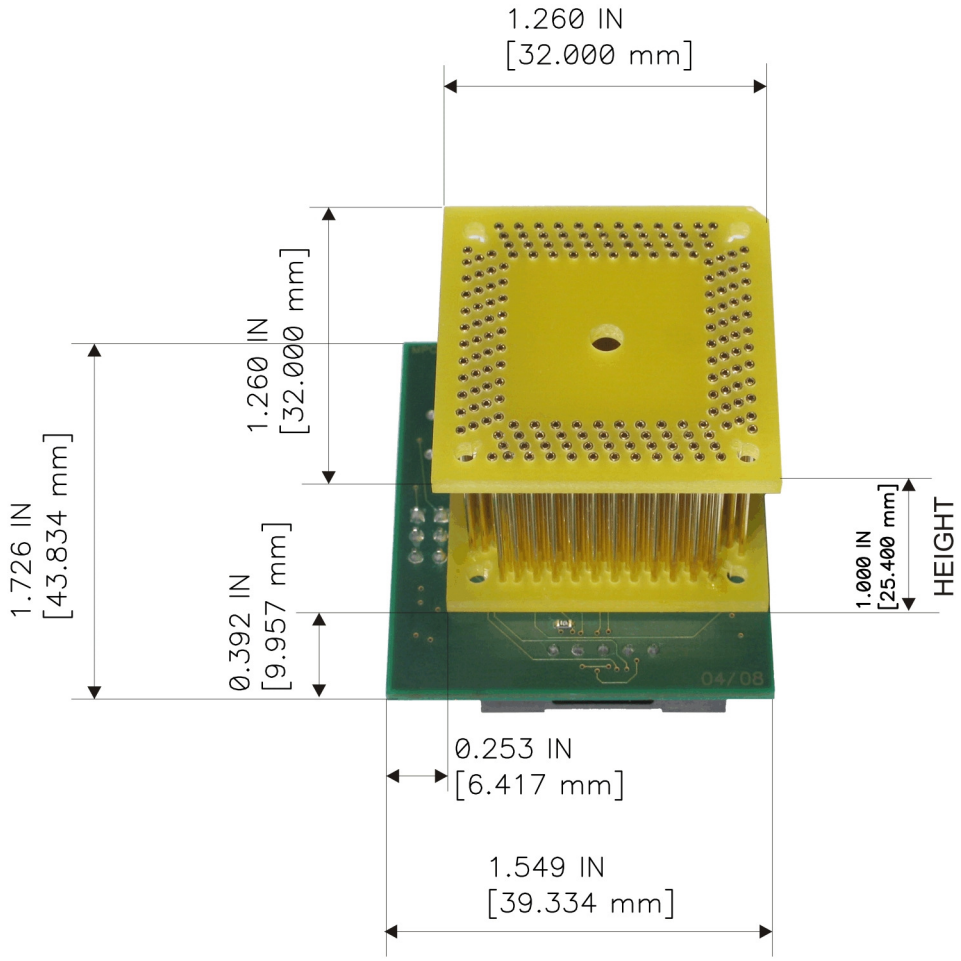
Jumper configuration

J1 and J2: clock source configuration

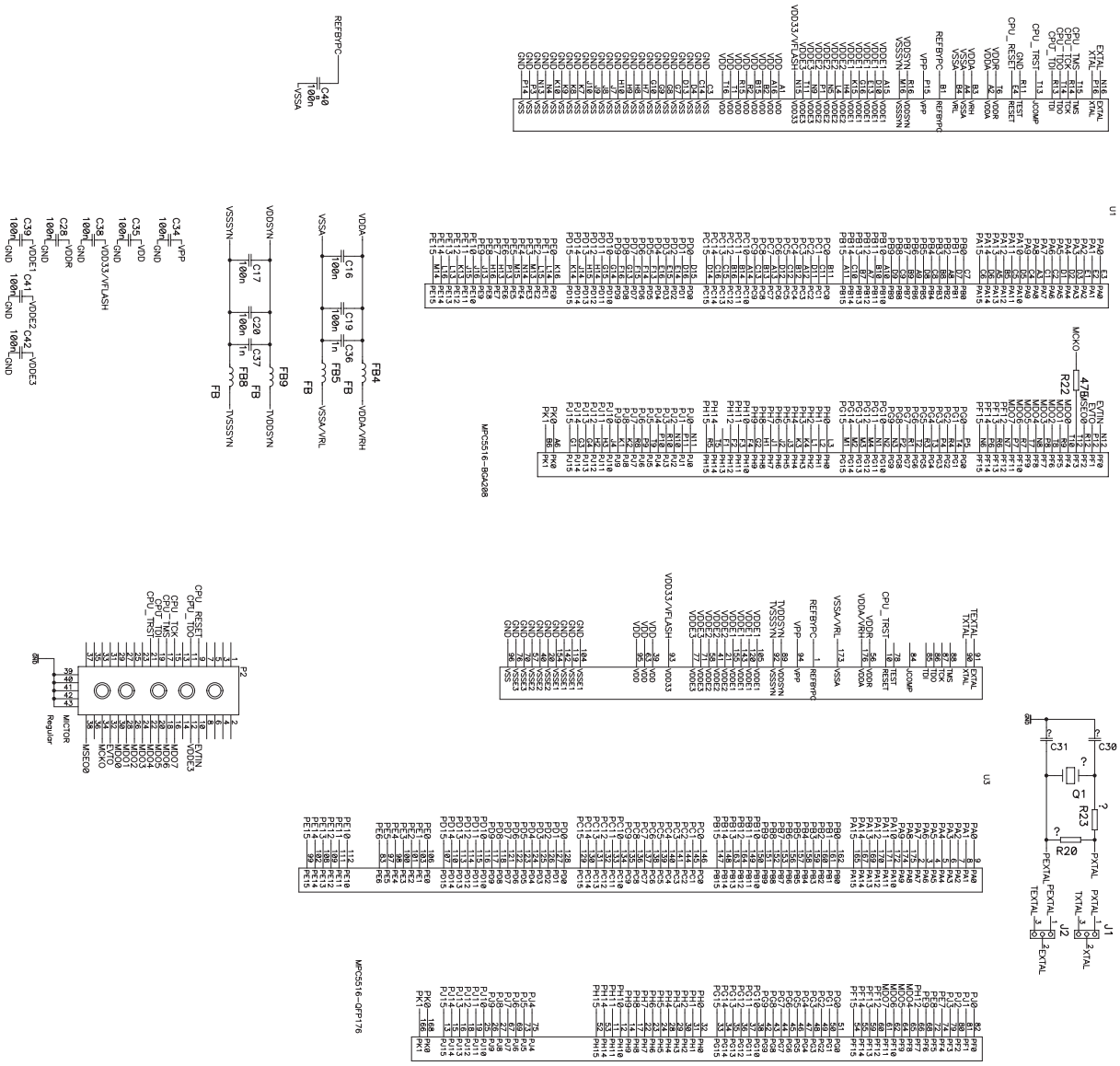


Jumpers J1 and J2 are used for clock source setting. When both jumpers are set to the position 1-2, the clock built on the Adapter is used and in this case, Q1, C30, C31, R20 and R23 must be populated. If the jumpers are set to 2-3, the clock from the target is used.

Dimensions



Schematic



* Schematic is the same for MPC5516 and MPC5517 Nexus Emulation Adapter.