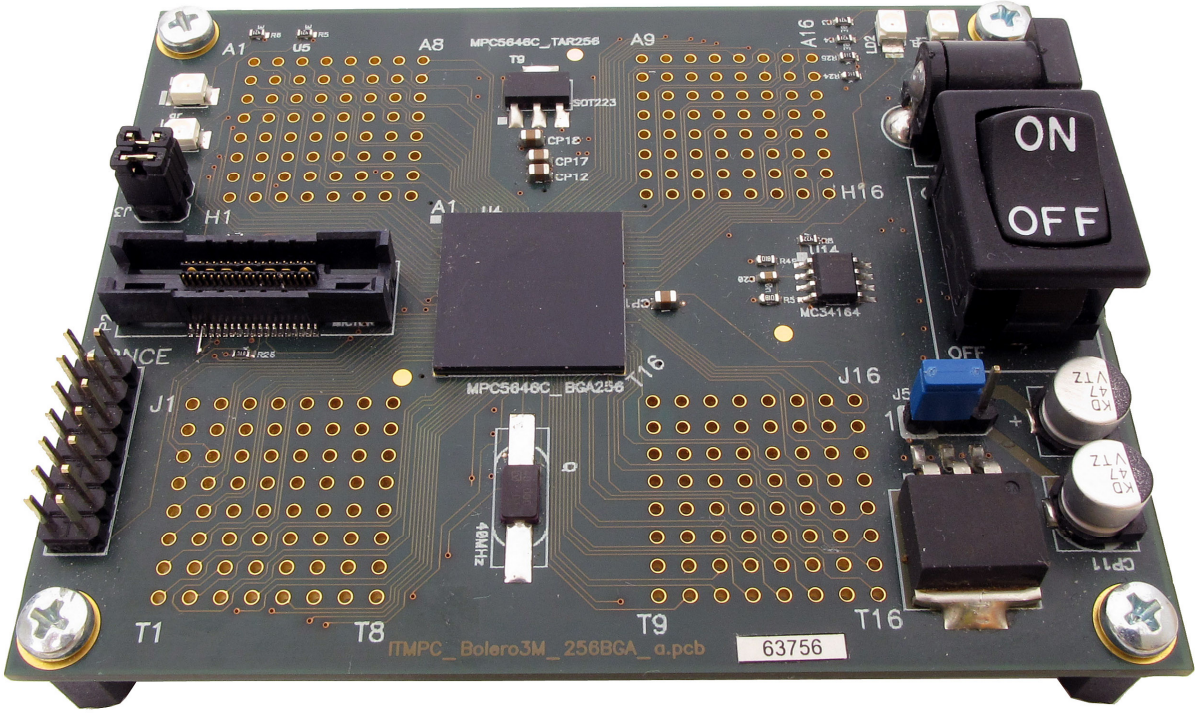
User's Manual

Freescale MPC5646C Target Board

	Ordering code
MPC5646C Target Board	**ITMPC5646C-256**



Solutions for Embedded Systems Development
www.isystem.com

Features

This target board is an evaluation and a development system for Freescale MPC5646C and ST SPC56EC74 microcontroller. The ITMPC5646C package features a target board populated with Freescale MPC5646C or ST SPC56EC74 CPU in the BGA256 package, ONCE debug and Nexus debug connector. A power supply also comes along with the board. The application under the development or test can run from the internal CPU flash or from the internal SRAM.

Specifications

Clock Speed – up to 120 MHz (e200z4d) and 80MHz (e200z0h)
Power requirement: 6 - 12V DC, + in the center @ 500 mA
Board Size: 106 mm x 86 mm

EVB-5646C Features

- MPC5646C or SPC56EC74, BGA256
- 40MHz clock (ext. crystal)
- Power Indicator – Supply voltage indication for 3.3/5V
- User Indicators – two LEDs connecting to the microcontroller
- Debug connections: ONCE (14-pin 2.54mm connector) and Nexus (Mictor 38-pin connector)

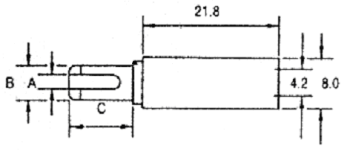
Software Development

The board has been tested with the microcontroller running at maximum frequency (120MHz). Software development can be performed by connecting the development tool to the ONCE (JTAG) or P4 (Nexus) connector. iSYSTEM provides various debug and test tools based on the iC5000 or the iC3000 unit. Contact iSYSTEM sales representative for more details on available tool options.

Power Supply

Permissible input voltage: 6-12 V DC, **+ in the center.** The required current load capacity of the power supply depends on the specific configuration of the target board. A power supply with a minimum of 500mA is recommended and delivered in the package. Low voltage DC plug must conform to the DIN 45323 standards:

- The hole diameter is 1.95 – 2.5 mm (standard: 2.1 mm)
- The external diameter is 6.2 - 5.5 mm (standard: 5.5 mm)



Dimensions

A	B	C
2.1	5.5	9.5

Switch-on the target board after the AC power supply is plugged into the wall and connected to the target board. Check that power indicator (LD1) lits, indicating that the voltage is present.

Note: When connecting an external debugger, make sure that the debugger is powered on first, then the target board and vice versa when switching off the system. First, switch off the target and then the emulator.

Settings and Options

Jumpers

Jumper J2 connects user LD4 LED to the MPC5646C pin G4 and jumper J3 connects user LD3 LED to the pin F3.

Jumper J5 selects power supply voltage for the CPU. The CPU is powered with 3.3V when the jumper is in the position 1-2 and with 5V when in the position 2-3.

Status Indicators

LD1 LED indicates a presence of the power supply voltage. It lits when the power is applied to the evaluation board and the power switch is switched on.

LD2 LED indicates reset line status.

LD3 and LD4 are available for the user.

Component List

Name	Description
U1	Motorola MPC5646C CPU
P2	Nexus debug connector
P3	Power supply connector
ONCE	JTAG debug connector
J2	Connects LD4 to CPU G4
J3	Connects LD3 to CPU F3
J5	Selects CPU power supply voltage
LD1	Power LED 3,3V
LD2	Reset indication LED
LD3	User LED
LD4	User LED
SW1	Power switch

Connectors

14-pin 2.54mm ONCE debug connector

CPU_TDI	**1**	**2**	GND
CPU_TDO	**3**	**4**	GND
CPU_TCK	**5**	**6**	GND
N.C.	**7**	**8**	N.C.
CPU_RESET	**9**	**10**	CPU_TMS
3V3	**11**	**12**	N.C.
N.C.	**13**	**14**	CPU_TRST

Mictor 38-pin Nexus debug connector

Signal	Pin	Pin	Signal
NC	1	2	NC
NC	3	4	NC
MD09	5	6	NC
NC	7	8	MDO8
RSTIN	9	10	EVTIN
TDO	11	12	VTREF
MDO10	13	14	NC
TCK	15	16	MDO7
TMS	17	18	MDO6
TDI	19	20	MDO5
NTRST	21	22	MDO4
MDO11	23	24	MDO3
NC	25	26	MDO2
NC	27	28	MDO1
NC	29	30	MDO0
NC	31	32	EVTO
NC	33	34	MCKO
NC	35	36	MSEO1
NC	37	38	MSEO0

Note: External debug tool must connect to one debug connector only! Only Mictor 38-pin connector exposes Nexus debug interface.

CPU expansion connection

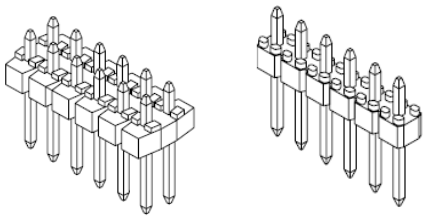
The target board exposes all MPC5646C pins/signals, which allow easy expansion of the development system.

The expansion array uses the same numbering scheme as the original microcontroller in the BGA256 package and also matches with the MPC5646C BGA256 pinout.

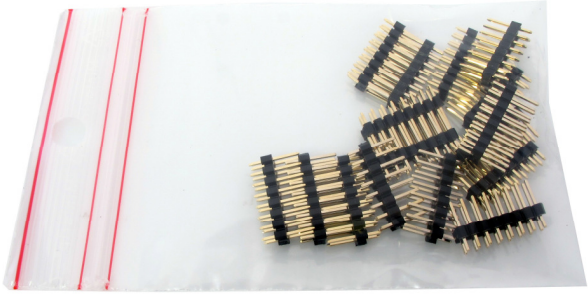
The target board can also act as a CPU module connecting to another custom tailored board by populating the expansion array with 2.54mm pitch headers on the bottom side.

For signal access and measurement the expansion array should be populated on the top side.

An example of breakaway dual and single row 2.54mm pitch headers, which can be easily stacked side-to-side:



A small plastic bag with headers comes along the target board already.



Appendix A

View of the ITMPC5646C

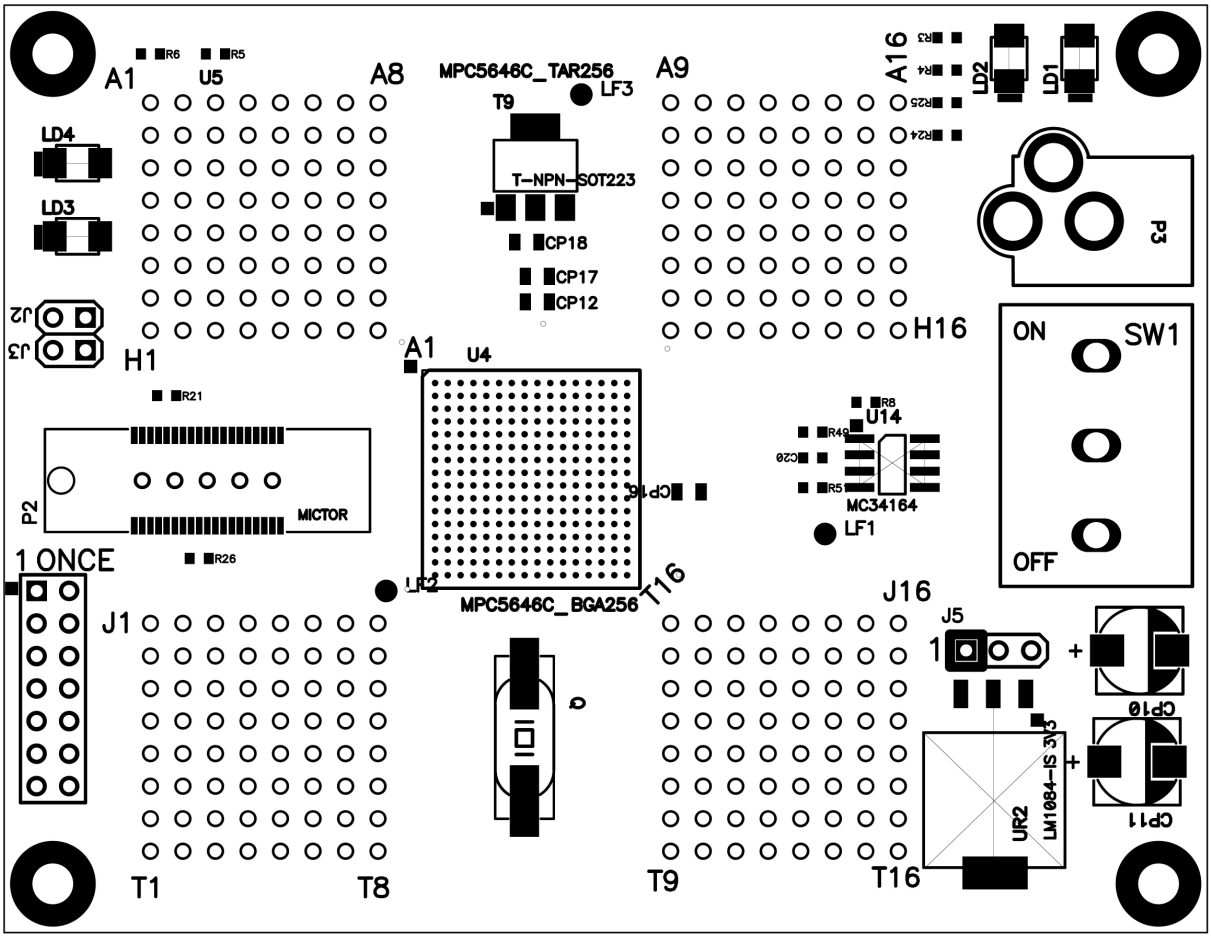


Figure 1

Note: A designation stands for A1 designation on the above ITMPC5646C view, B stands for B1, etc.

Expansion Connection as seen from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[15]	PB[2]	PC[13]	PI[1]	PE[7]	PH[8]	PE[2]	PE[4]	PC[4]	PE[3]	PH[9]	PI[4]	PH[11]	PE[14]	PA[10]	PG[11]	A
B	PH[13]	PC[14]	PC[8]	PC[12]	PI[3]	PE[6]	PH[5]	PE[5]	PC[5]	PC[0]	PC[2]	PH[12]	PG[10]	PA[11]	PA[9]	PA[8]	B
C	PH[14]	VDD_HV_A	PC[9]	PL[0]	PI[0]	PH[7]	PH[6]	VSS_LV	VDD_HV_A	PA[5]	PC[3]	PE[15]	PG[14]	PE[12]	PA[7]	PE[13]	C
D	PG[5]	PI[6]	PJ[4]	PB[3]	PK[15]	PI[2]	PH[4]	VDD_LV	PC[1]	PH[10]	PA[6]	PI[5]	PG[15]	PF[14]	PF[15]	PH[2]	D
E	PG[3]	PI[7]	PH[15]	PG[2]	VDD_LV	VSS_LV	PK[10]	PK[9]	PM[1]	PM[0]	PL[15]	PL[14]	PG[0]	PG[1]	PH[0]	VDD_HV_A	E
F	PA[2]	PG[4]	PA[1]	PE[1]	PL[2]	PM[6]	PL[1]	PK[11]	PM[5]	PL[13]	PL[12]	PM[2]	PH[1]	PH[3]	PG[12]	PG[13]	F
G	PE[8]	PE[0]	PE[10]	PA[0]	PL[3]	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[12]	VDD_HV_B	PI[13]	PI[12]	PA[3]	G
H	PE[9]	VDD_HV_A	PE[11]	PK[1]	PL[4]	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	VSS_HV	PK[13]	VDD_HV_A	VDD_LV	VSS_LV	PI[11]	H
J	VSS_HV	VRC_CTRL	VDD_LV	PG[9]	PL[5]	VSS_LV	VSS_LV	VSS_LV	VSS_HV	VSS_HV	VSS_HV	PK[14]	PD[15]	PI[8]	PI[9]	PI[10]	J
K	RESET	VSS_LV	PG[8]	PC[11]	PL[6]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[3]	PD[14]	PD[13]	PB[14]	PB[15]	K
L	PC[10]	PG[7]	PB[0]	PK[2]	PL[7]	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV	VDD_LV	PM[4]	PD[12]	PB[12]	PB[13]	VDD_HV_ADC1	L
M	PG[6]	PB[1]	PK[4]	PF[9]	PK[5]	PK[6]	PK[7]	PK[8]	PL[8]	PL[9]	PL[10]	PL[11]	PB[11]	PD[10]	PD[11]	VSS_HV_ADC1	M
N	PK[3]	PF[8]	PC[6]	PC[7]	PJ[13]	VDD_HV_A	PB[10]	PF[6]	VDD_HV_A	PJ[1]	PD[2]	PJ[5]	PB[5]	PB[6]	PJ[6]	PD[9]	N
P	PF[12]	PF[10]	PF[13]	PA[14]	PJ[9]	PA[12]	PF[0]	PF[5]	PF[7]	PJ[3]	PI[15]	PD[4]	PD[7]	PD[8]	PJ[8]	PJ[7]	P
R	PF[11]	PA[15]	PJ[11]	PJ[15]	PA[13]	PF[2]	PF[3]	PF[4]	VDD_LV	PJ[2]	PJ[0]	PD[0]	PD[3]	PD[6]	VDD_HV_ADC0	PB[7]	R
T	PJ[12]	PA[4]	PK[0]	PJ[14]	PJ[10]	PF[1]	XTAL	EXTAL	VSS_LV	PB[9]	PB[8]	PI[14]	PD[1]	PD[5]	VSS_HV_ADC0	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 2

Schematic