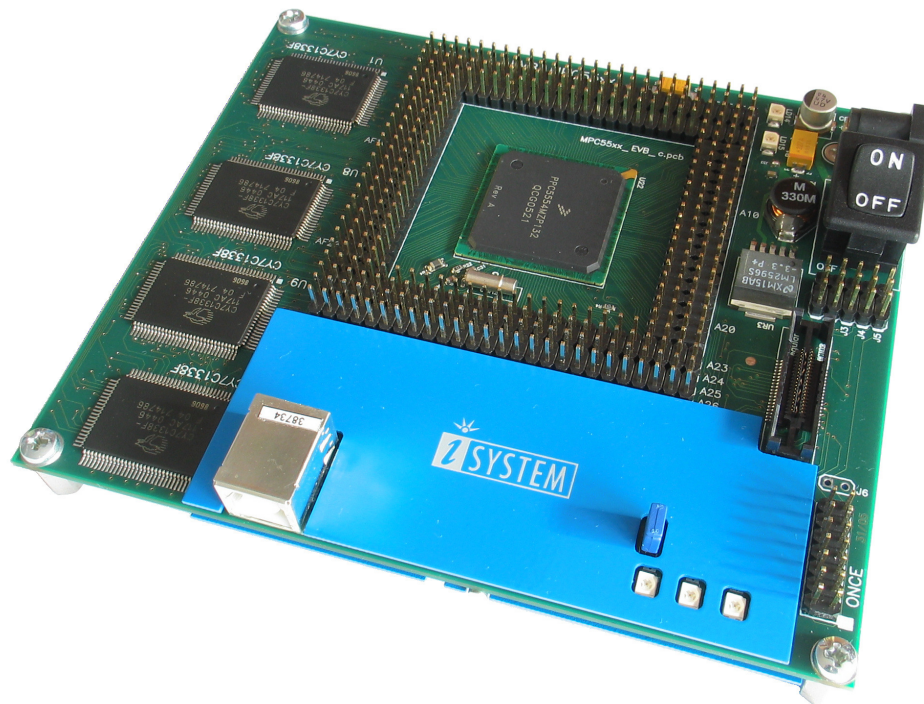


## EVB-5567 Evaluation & Development Kit for Freescale PowerPC MPC5567 Microcontroller

	Ordering code
EVB-5567	ITMPC5567



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## Features

The ITMPC5567 Target Board is an evaluation and a development system for the Freescale MPC5567 microcontroller. The ITMPC5567 package consists of a USB cable, a power supply and a target board populated with the Freescale MPC5567 CPU, option of installation of 2 MB SRAM (4 devices 128Kx32-bit, not populated), JTAG debug and Nexus debug connectors and an on-board integrated iSYSTEM JTAG debugger. The application under the development or test runs from the internal CPU flash.

## Specifications

Clock Speed – up to 132 MHz

Power requirement: 6 - 12V DC , + in the center @ 500 mA

Power output: 5V, 3.3V, and 2.5V regulated supplies

Board Size: 131 mm x 110 mm

## EVB-5567 Features

- MPC5567
- Optional ext. 2Mbit (4 devices 128K x 32-bit) SRAM (CY7C1338F) – not populated
- 8MHz clock (ext. crystal)
- Power Indicators – Supply voltage indications for 5V, 3.3V, and 2.5V supplies
- User Indicator – two user indicators to provide user conceived visual response during testing
- Configuration jumper - Jumpers J1 to J5 configures processor startup mode; Jumper J6 enables/disables the iSYSTEM on-board integrated USB-JTAG debugger
- Two debug options available – JTAG, Nexus
- Low cost and user friendly support manual and software

## Software Development

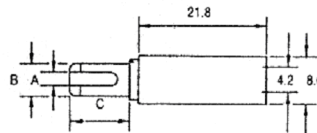
The board has been tested and does run at speeds up to 132 MHz, which you can set by engaging the PLL module in your software. Software development on the EVB-5567 can be performed using the iSYSTEM on-board integrated USB-JTAG debugger. Alternatively, external development tools can be connected to the ONCE (JTAG) or P2 (Nexus) connector. This provides real-time access to all hardware, peripherals and memory on the board. Software is usually uploaded to the external SRAM where it's executed during the development. Then it can be programmed into the CPU Flash in order to execute in standalone when the power is applied.

## Getting Started - Setting up the EVB-5567 Board

### Power Supply

Permissible input voltage: 6-12 V DC, **+ in the center**. The required current load capacity of the power supply depends on the specific configuration of the ITMPC5567. A power supply with a minimum of 500mA is recommended and delivered in the package. Low voltage DC plug must conform to the DIN 45323 standards:

- The hole diameter is 1.95 – 2.5 mm (standard: 2.1 mm)
- The external diameter is 6.2 - 5.5 mm (standard: 5.5 mm)



Dimensions

A	B	C
2.1	5.5	9.5

Switch-on the EVB-5567 after the AC adapter is plugged into the wall and connected to the EVB-5567. Check that power indicators (LD11, LD12, LD13) lit, indicating that 5V, 3.3V and 2.5V voltage is present.

---

Note: When connecting an external debugger, make sure that the emulator is powered on first, then the target board and vice versa when switching off the system. First, switch off the target and then the emulator.

---

## Use of On-Board Integrated Debugger

Follow below instructions, in order to get a sample application running with “out of the box” experience.

If winIDEA 2006 CD is not part of the package, please obtain winIDEA 2006 setup from your local iSYSTEM office or from [www.isystem.com](http://www.isystem.com).

- Install winIDEA 2006 (IDE) full setup on a PC.
- Set jumpers J1-J5 in their default position.
- Set jumper J6, which enables on-board integrated debugger.
- Make sure that power switch on the ITMPC5567 is in off position.
- Connect the power supply to the ITMPC5567.
- Switch on the ITMPC5567.
- Run winIDEA by selecting Start>Programs>... and open ITMPC5567 sample workspace (.jrf) running from the internal flash c:\winIDEA\2006\Examples\Targets\ITMPC5567\IntFLASH).
- Connect USB cable between the PC and the ITMPC5567.
- Windows should auto-detect a new USB device and install belonging USB driver. In case of any problems, the driver is located under winIDEA install directory (e.g. c:\winIDEA\2006\USBDrv).
- Execute Debug/Download. This should program and run the application until main function.
- The application is now ready for debugging. If you run the application, a successful operation is indicated with blinking LED LD11 and LD12.

---

The on-board integrated USB-JTAG debugger runs without restrictions for 90 days after using it for the first time. After the 90 day period expires, the debugger falls back to a restriction of a 32k byte download limit.

The debugger can be upgraded to a regular debugger (no limits) by purchasing the debug enable license. Additionally, you need to purchase a regular winIDEA license. Please contact your local iSYSTEM distributor for more details on upgrading your development tool.

---

## What To Do Now?

winIDEA allows you to run code step by step, set execution and access breakpoints, examine and modify the source code, rebuild the project using GNU compiler, which is optionally installed during winIDEA installation, and much more. For more information refer to the winIDEA documentation. Software in the combination with the development board can be used as a basis for developing future applications also on your hardware. This project illustrates various programming issues, which are essential to all winIDEA projects:

- Initialization of bus interface unit
- Initialization of configuration registers
- Implementation of dispatch table
- Format of linker definition file
- Correct project settings (Project>Settings), which ensure that the compiler is invoked successfully

More interesting examples are also included on the support CD.

## Troubleshooting

### **EVB-5567 doesn't show signs of life by first start**

- a) Check the power supplied to the EVB board – Diodes LD11, LD12 and LD13.
- b) When using the on-board integrated JTAG debugger, make sure that Jumper J6 is enabled. When Jumper J6 is not enabled, a connection to the JTAG or Nexus port must be made.
- c) Try “slow” JTAG Scan Speed if the debugger cannot connect to the CPU.
- d) Execute debug Reset instead of debug Download.

### **Unable to download the code to the board**

- a) Check the power supplied to the EVB board.
- b) Ensure that the correct workspace was loaded into winIDEA.
- c) Check the hardware configuration:
  - Tools>Hardware Plug-In
  - Hardware>Hardware ...
  - Hardware>Emulation Options
- d) Reset the board and try to connect again.

### **Checksum failed error**

- a) When performing any kind of checksum, remove all software breakpoints

## **Default Memory Map**

The MPC5567 of the MPC5500 family has two levels of memory hierarchy. The fastest accesses are to the unified 32 Kbytes cache. The next level in the hierarchy contains the 96-Kbyte internal SRAM and internal 2MB Flash memory. Both the internal SRAM and the Flash memory can hold instructions and data. The external bus interface has been designed to support most of the standard memories used with the MPC55xx family. The provided software uses the default memory map. If you modify the memory map make sure that all memory banks and chip select configuration settings are adjusted accordingly.

## EVB-5567 Memory Map

### Internal Memory

Address Range	Memory Type	Description
0x 0000 0000- 0x 001F FFFF	2MB - Internal Flash Memory	Internal Flash memory (512KB – 2MB)
0x 2000 0000- 0x 3FFF FFFF	512MB - External Memory	External Memory (see note below)
0x 4000 0000- 0x 4000 7FFF	Internal SRAM, Powered Standby	32 Kbytes
0x 4000 8000- 0x 4000 FFFF	Internal SRAM	32 Kbytes

### External Memory

There are 4 SRAM devices connected to CS1 and CS2 and cover a 2MB memory area. Offset depends on the CPU configuration. In our case, CS1 is configured to point at 0x2000 0000 through the winIDEA initialization sequence.

Address Range
0x 2000 0000 – 0x 2007 FFFF
0x 2008 0000 – 0x 200F FFFF
0x 2010 0000 – 0x 2017 FFFF
0x 2018 0000 – 0x 201F FFFF

### SRAM Memory

The MPC5567 internal SRAM module provides a general-purpose 64-Kbyte memory block that supports mapped read/write accesses from any master. Included within the 64-Kbyte SRAM block is a 32-Kbyte block powered by a separate supply for a standby operation.

### Flash Memory

The MPC5567 provides 2 Mbytes of programmable, non-volatile, Flash memory storage. The non-volatile memory (NVM) can be used for instruction and/or data storage.

### Downloading the code into the memory

winIDEA allows you to load the code directly into the internal Flash memory through the standard debug download. winIDEA identifies, which code from the download file fits in the internal FLASH, and loads it to the Flash through the flash programming procedure hidden to the user. All other code propagates to the target through standard memory writes.

Demo software has the example configured for the internal Flash. Load the project into winIDEA and execute debug download (Debug->Download), which will download the code directly to the Flash memory. For more information see the winIDEA users manual.

Demo software has also the example configured for the optionally populated external SRAM. Load the project into winIDEA and execute debug download (Debug->Download), which will download the code to the external SRAM. Access to the external SRAM is configured in the initialization sequence ('Hardware/Emulation Options/Initialization' tab), which winIDEA executes prior to debug download.

## Settings and Options

### Jumpers

Jumpers J1 to J5 configures processor startup mode. See MPC5567 Reference Manual for more details on the CPU signals BOOTCFG[0:1], PLLCFG[0:1] and WKPCFG. Some boards may not have J1-J5 populated since the CPU has internal pull-ups/downs on belonging signals, which match with the default jumper settings. Jumper J6 selects whether iSYSTEM on-board integrated USB-JTAG debugger is used or an external debug tool.

Jumper pin 1 is marked with a white square on the ITMPC5567 PCB. If pin 1 cannot be located directly from the ITMPC5567, please use Figure 2 for assistance.

**Note:** Don't change jumper settings while the ITMPC5567 Target Board is supplied with power!

<b>J1</b>	<b>BOOTCFG0</b>
1-2*	BOOTCFG0 = 0
2-3	BOOTCFG0 = 1
<b>J2</b>	<b>BOOTCFG1</b>
1-2*	BOOTCFG1 = 0
2-3	BOOTCFG1 = 1
<b>J3</b>	<b>PLLCFG0</b>
1-2	PLLCFG0 = 0
2-3*	PLLCFG0 = 1
<b>J4</b>	<b>PLLCFG1</b>
1-2	PLLCFG1 = 0
2-3*	PLLCFG1 = 1
<b>J5</b>	<b>WKPCFG</b>
1-2	WKPCFG = 0
2-3*	WKPCFG = 1
<b>J6</b>	<b>Debug mode</b>
Closed*	Enable integrated USB-JTAG debugger
Open	External debugger

Figure 1: Jumper configuration (\* - default position)

## Status Indicators

Three LED diodes show the presence of supply voltages. LD11 (+5V), LD12 (+3.3V) and LD13 (+2.5V) must light when the power is applied to the evaluation board. LD14 and LD15 are available for the user as a status indicator.

## Component List

Name	Description
U22	Motorola MPC5567 CPU
U1,U8,U9,U10	SRAM Cypress CY7C1338F
P1(bottom)	Connector for manufacturing purpose
P2	Nexus debug connector
P4	Power supply connector
ONCE	JTAG debug connector
J1	BOOTCFG0
J2	BOOTCFG1
J3	PLLCFG0
J4	PLLCFG1
J5	WKPCFG
J6	Debug mode
J28	USB connector (integrated debugger)
LD11	Power LED 5V
LD12	Power LED 3,3V
LD13	Power LED 2,5V
LD14	User LED
LD15	User LED
SW1	Power switch

## Connectors

### 14-pin JTAG debug connector (ONCE)

CPU_TDI	1	2	GND
CPU_TDO	3	4	GND
CPU_TCK	5	6	GND
N.C.	7	8	N.C.
CPU_RESET	9	10	CPU_TMS
3V3	11	12	N.C.
N.C.	13	14	CPU_TRST

External JTAG debug tool connects to a 14-pin JTAG debug connector. **Jumper J6 must be open when using external debugger.**

## Nexus 38-pin Mictor debug connector

Signal	Pin	Pin	Signal
Not used	1	2	Not used
Not used	3	4	Not used
MDO9	5	6	CLKOUT
BOOTCFG	7	8	MDO8
RSTIN	9	10	EVTIN
TDO	11	12	VTREF
MDO10	13	14	RDY
TCK	15	16	MDO7
TMS	17	18	MDO6
TDI	19	20	MDO5
NTRST	21	22	MDO4
MDO11	23	24	MDO3
Not used	25	26	MDO2
Not used	27	28	MDO1
Not used	29	30	MDO0
Not used	31	32	EVTO
Not used	33	34	MCKO
Not used	35	36	MSEO1
Not used	37	38	MSEO0

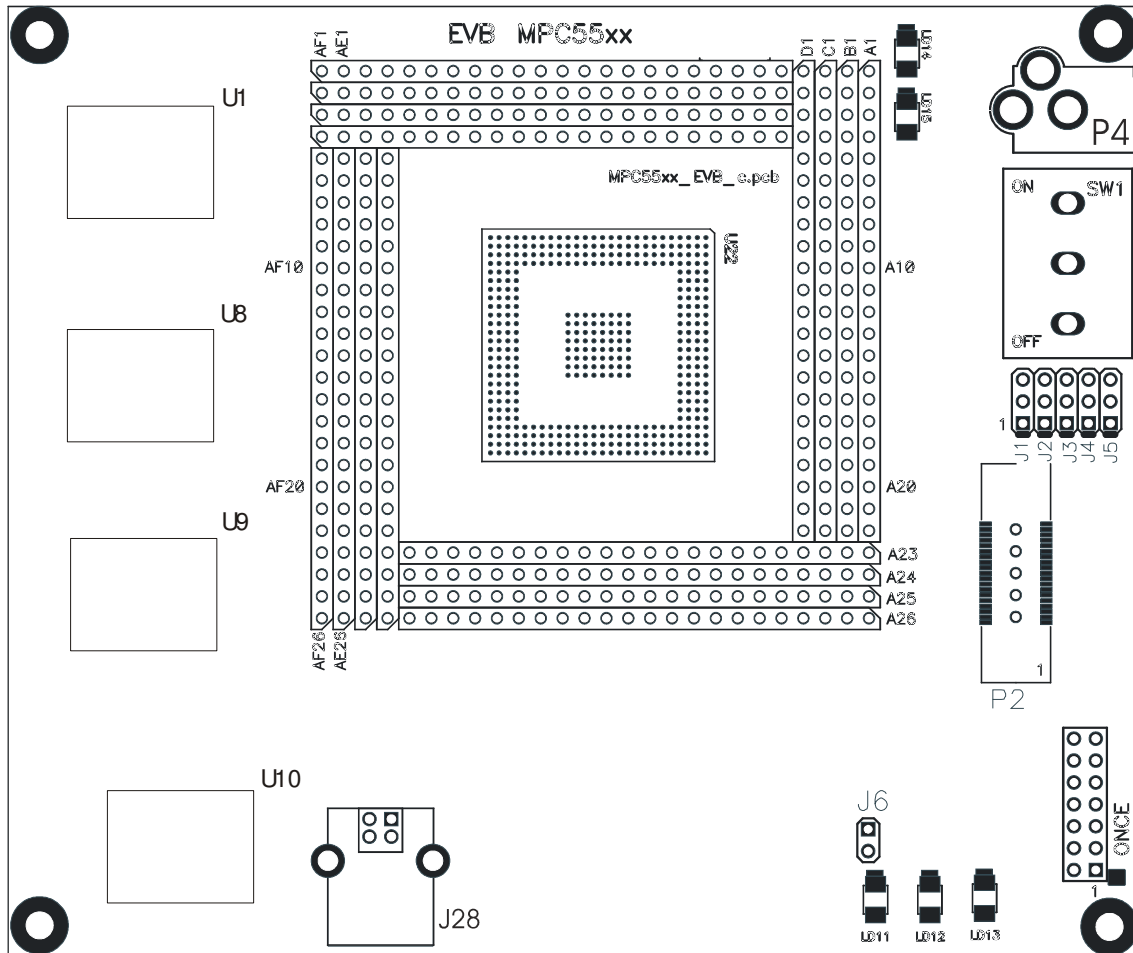
External Nexus debug tool connects to a Nexus 38-pin Mictor debug connector. **Jumper J6 must be open when using external debugger.**

### CPU expansion connector

The CPU expansion connector makes all the CPU signals accessible and can be used in order to expand the development system by connecting the ITMPC5567 to another module. The CPU expansion connector uses the same numbering scheme as the original CPU in the PBGA416 package. The CPU expansion connector builds the matrix that matches with the CPU PBGA416 pinout.

# Appendix A

## View of the ITMPC5567



Note: A designation on *Figure 4* stands for A1 designation on the above ITMPC5567 view, B stands for B1, AF stands for AF1 etc.

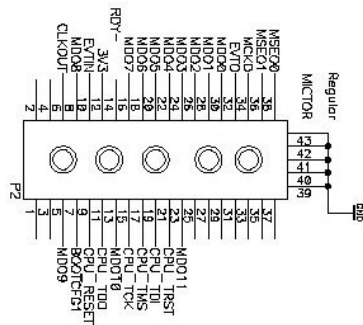
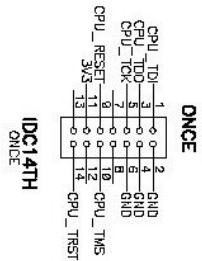
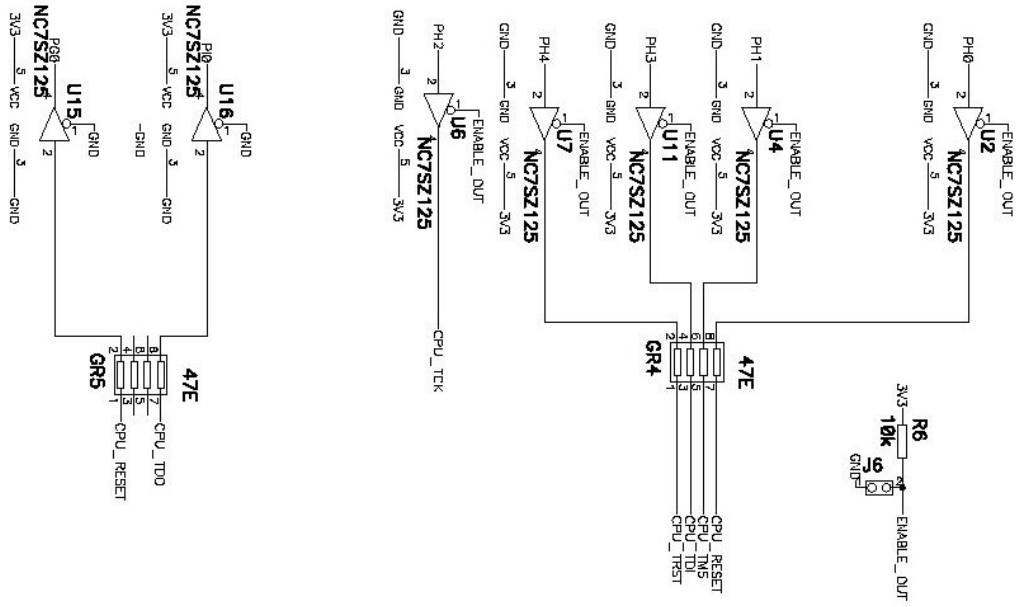
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	V <sub>SS</sub>	V <sub>SBY</sub>	AN37	AN11	V <sub>DDA</sub>	AN16	AN1	AN5	VRH	AN23	AN27	AN28	AN35	V <sub>SS</sub>	AN15	ETRG1	ETPUB18	ETPUB20	ETPUB24	ETPUB27	MDO11	MDO8	V <sub>DD</sub>	V <sub>DD33</sub>	V <sub>SS</sub>
B	V <sub>DD</sub>	V <sub>SS</sub>	AN36	AN39	AN19	AN20	AN0	AN4	BIASR	AN22	AN26	AN31	AN32	V <sub>SS</sub>	AN14	ETRG0	ETPUB21	ETPUB25	ETPUB38	ETPUB31	MDO7	MDO4	MDO0	V <sub>SS</sub>	
C	V <sub>DD33</sub>	V <sub>DD</sub>	V <sub>SS</sub>	AN8	AN17	V <sub>SSA</sub>	AN21	AN3	AN7	VRL	AN25	AN30	AN33	V <sub>DDHB9</sub>	AN13	ETPUB19	ETPUB22	ETPUB26	ETPUB30	MDO6	MDO1	V <sub>SS</sub>	V <sub>DDH7</sub>	V <sub>DD</sub>	
D	ETPUA30	ETPUA31	V <sub>DD</sub>	V <sub>SS</sub>	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34	V <sub>DDHB9</sub>	AN12	ETPUB16	ETPUB17	ETPUB23	ETPUB29	MDO2	V <sub>DDHB8</sub>	V <sub>DDH7</sub>	TCK	TDI	
E	ETPUA28	ETPUA29	V <sub>DDHB1</sub>	V <sub>DD</sub>																		TMS	TD0	TEST	
F	ETPUA24	ETPUA27	ETPUA26	V <sub>DDHB1</sub>																		JCOMP	EVTI	EVTO	
G	ETPUA23	ETPUA22	ETPUA25	ETPUA21																		MCKO	GPIO204	ETPUB15	
H	ETPUA20	ETPUA19	ETPUA18	ETPUA17																		GPIO203	ETPUB14	ETPUB13	
J	ETPUA16	ETPUA15	ETPUA14	ETPUA13																		RDY	ETPUB12	ETPUB9	
K	ETPUA12	ETPUA11	ETPUA10	ETPUA9																		V <sub>DDHB6</sub>	ETPUB11	ETPUB8	
L	ETPUA8	ETPUA7	ETPUA6	ETPUA5																		ETPUB10	ETPUB8	ETPUB7	
M	ETPUA4	ETPUA3	ETPUA2	ETPUA1																		ETPUB6	ETPUB4	ETPUB3	
N	BDIP	TEX	ETPUA0	TCRCLK																		TCRCLK	ETPUB1	SINB	
P	CS3	CS2	CS1	CS0																		SOUTB	PCSB3	PCSB0	
R	WE3	WE2	WE1	WE0																		PCSA3	PCSB4	SCKB	
T	V <sub>DDH7</sub>	TSIZ0	RD_WK	V <sub>DDH7</sub>																		PCSA1	PCSA0	PCSA2	
U	ADDR16	TSIZ1	TA	V <sub>DD33</sub>																		PCSA4	TXDA	PCSA5	
V	ADDR18	ADDR17	TS	ADDR8																		CNTXC	RXDA	RSTOUT	
W	ADDR20	ADDR19	ADDR9	ADDR10																		RXDB	CNRXC	TXDB	
Y	ADDR22	ADDR21	ADDR11	V <sub>DDH7</sub>																		WRKCFG	BOOTCFG1	V <sub>RCVSS</sub>	
AA	ADDR24	ADDR23	ADDR13	ADDR12																		V <sub>DDH6</sub>	PLLCFG1	BOOTCFG0	
AB	V <sub>DDH7</sub>	ADDR25	ADDR15	ADDR14																		V <sub>DD</sub>	V <sub>RCCTL</sub>	PLLCFG0	
AC	ADDR26	ADDR27	ADDR31	V <sub>SS</sub>	V <sub>DD</sub>	DATA26	DATA28	V <sub>DDH7</sub>	DATA30	DATA31	DATA28	DATA10	DATA12	DATA14	EMIOS2	EMIOS8	EMIOS12	EMIOS21	V <sub>DDHB4</sub>	V <sub>DDH5</sub>	NC	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>RC33</sub>	
AD	ADDR28	ADDR30	V <sub>SS</sub>	V <sub>DD</sub>	DATA24	DATA25	DATA27	DATA29	V <sub>DD33</sub>	GPIO 207	DATA9	DATA11	DATA13	DATA15	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS17	EMIOS22	CNTXA	NC	V <sub>SS</sub>	V <sub>DD</sub>	
AE	ADDR29	V <sub>SS</sub>	V <sub>DD</sub>	DATA17	DATA19	DATA21	DATA23	DATA0	DATA2	DATA4	DATA6	OE	BE	BE	EMIOS5	EMIOS9	EMIOS13	EMIOS16	EMIOS19	EMIOS23	CNRXA	V <sub>DDH7</sub>	CLKOUT	V <sub>SS</sub>	
AF	V <sub>SS</sub>	V <sub>DD</sub>	DATA18	DATA16	DATA20	DATA22	DATA22	GPIO 206	DATA1	DATA3	V <sub>DDH7</sub>	DATA5	DATA7	BB	EMIOS6	EMIOS4	EMIOS7	EMIOS11	EMIOS14	EMIOS18	EMIOS20	CNTXB	V <sub>DDH7</sub>	ENGLCK	V <sub>SS</sub>

(As viewed from the top of the package)

Figure 4: Expansion connector

# Schematic

Note: On-board integrated JTAG debugger is not part of the schematic.



CPU_RESET	WLS_RESET
HE10013	AD00
HE10014	AD01
HE10015	AD02
HE10016	AD03
HE10017	AD04
HE10018	AD05
HE10019	AD06
HE10020	AD07
HE10021	AD08
HE10022	AD09
HE10023	AD10
HE10024	AD11
HE10025	AD12
HE10026	AD13
HE10027	AD14
HE10028	AD15
HE10029	AD16
HE10030	AD17
HE10031	AD18
HE10032	AD19
HE10033	AD20
HE10034	AD21
HE10035	AD22
HE10036	AD23
HE10037	AD24
HE10038	AD25
HE10039	AD26
HE10040	AD27
HE10041	AD28
HE10042	AD29
HE10043	AD30
HE10044	AD31
HE10045	AD32
HE10046	AD33
HE10047	AD34
HE10048	AD35
HE10049	AD36
HE10050	AD37
HE10051	AD38
HE10052	AD39
HE10053	AD40
HE10054	AD41
HE10055	AD42
HE10056	AD43
HE10057	AD44
HE10058	AD45
HE10059	AD46
HE10060	AD47
HE10061	AD48
HE10062	AD49
HE10063	AD50
HE10064	AD51
HE10065	AD52
HE10066	AD53
HE10067	AD54
HE10068	AD55
HE10069	AD56
HE10070	AD57
HE10071	AD58
HE10072	AD59
HE10073	AD60
HE10074	AD61
HE10075	AD62
HE10076	AD63
HE10077	AD64
HE10078	AD65
HE10079	AD66
HE10080	AD67
HE10081	AD68
HE10082	AD69
HE10083	AD70
HE10084	AD71
HE10085	AD72
HE10086	AD73
HE10087	AD74
HE10088	AD75
HE10089	AD76
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HE10208	AD195
HE10209	AD196
HE10210	AD197
HE10211	AD198
HE10212	AD199
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1A		1B		1C		1D	
NET00078	1	3V3	1	VDD	1	GND	1
NET00079	2	VDD	2	GND	2	GND	2
VDD	3	GND	3	NET00045	3	NET00015	3
GND	4	NET00064	4	NET00046	4	NET00044	4
NET00080	5	NET00065	5	NET00048	5	5V	5
NET00081	6	GND	6	NET00049	6	NET00019	6
NET00082	7	NET00066	7	NET00050	7	NET00028	7
NET00083	8	NET00067	8	NET00051	8	NET00030	8
NET00084	9	NET00069	9	BIASR	9	5V	9
NET00085	10	GND	10	NET00052	10	NET00033	10
NET00086	11	NET00070	11	NET00053	11	NET00034	11
NET00087	12	NET00071	12	NET00054	12	NET00036	12
NET00088	13	NET00072	13	NET00057	13	NET00036	13
5V	14	5V	14	GND	14	NET00036	14
NET00089	15	NET00073	15	NET00058	15	GND	15
NET00090	16	NET00074	16	NET00058	16	NET00037	16
NET00091	17	NET00075	17	NET00060	17	NET00038	17
NET00092	18	NET00076	18	NET00061	18	NET00040	18
NET00093	19	NET00077	19	NET00062	19	NET00041	19
MDO5	20	MDO9	20	NET00063	20	NET00042	20
MDO2	21	MDO6	21	NET00063	21	NET00043	21
5V	22	MDO3	22	MDO10	22	NET00044	22
				MDO7		MDO11	

2A		2B		2C		2D	
MDO8	1	VDD	1	3V3	1	GND	1
MDO4	2	MDO0	2	GND	2	3V3	2
MDO1	3	GND	3	3V3	3	VDD	3
GND	4	3V3	4	CPU_TCK	4	CPU_TDI	4
3V3	5	CPU_TMS	5	CPU_TDO	5	NET00084	5
MSEC0	6	CPU_TRST	6	EVTIN	6	EVTO	6
MSEC1	7	MCKD	7	LED2	7	NET00085	7
NET00096	8	LED1	8	NET00097	8	NET00098	8
5V	9	NET00099	9	NET00100	9	NET00101	9
NET00102	10	NET00103	10	NET00104	10	NET00105	10
NET00106	11	NET00107	11	NET00108	11	NET00109	11
NET00110	12	NET00111	12	NET00112	12	NET00113	12
NET00114	13	NET00115	13	NET00116	13	NET00117	13
NET00118	14	NET00119	14	NET00120	14	NET00121	14
NET00122	15	NET00123	15	NET00120	15	NET00126	15
NET00126	16	NET00127	16	NET00128	16	5V	16
NET00129	17	NET00130	17	NET00131	17	3V3	17
NET00132	18	NET00133	18	NET00134	18	RSTCFG	18
NET00138	19	NET00139	19	NET00140	19	CPU_RESET	19
WKPCFG	20	BOOTCFG1	20	GND	20	GND	20
5V	21	PLLCFG1	21	BOOTCFG0	21	EXTAL-	21
VDD	22	VRCCTL	22	PLLCFG0	22	XTAL-	22

3A		3B		3C		3D	
VDDSYN	1	3V3	1	VDD	1	GND	1
3V3	2	VDD	2	GND	2	NET00138	2
VDD	3	GND	3	CLKDUT	3	3V3	3
GND	4	NET00137	4	3V3	4	NET00135	4
NET00141	5	3V3	5	NET00142	5	NET00143	5
3V3	6	NET00144	6	NET00145	6	NET00146	6
5V	7	NET00147	7	NET00148	7	NET00149	7
NET00150	8	NET00151	8	NET00152	8	NET00153	8
NET00154	9	NET00155	9	NET00156	9	NET00157	9
NET00158	10	NET00159	10	NET00160	10	NET00161	10
NET00162	11	NET00163	11	NET00164	11	NET00165	11
DATA14	12	NET00167	12	NET00168	12	NET00169	12
DATA12	13	DATA15	13	NET00172	13	NET00173	13
3V3	14	DATA13	14	NET00176	14	DATA7	14
DATA10	15	DATA11	15	ED	15	DATA5	15
DATA8	16	DATA9	16	DATA6	16	3V3	16
DATA31	17	NET00203	17	DATA4	17	DATA3	17
DATA30	18	3V3	18	DATA2	18	DATA1	18
3V3	19	DATA29	19	DATA0	19	NET00198	19
DATA28	20	DATA27	20	DATA23	20	DATA22	20
DATA26	21	DATA25	21	DATA21	21	DATA20	21
VDD	22	DATA24	22	DATA19	22	3V3	22

4A		4B		4C		4D	
DATA18	1	DATA16	1	VDD	1	GND	1
DATA17	2	VDD	2	GND	2	ADD20	2
VDD	3	GND	3	ADD30	3	ADD28	3
GND	4	ADD31	4	ADD27	4	ADD26	4
ADD14	5	ADD15	5	ADD25	5	3V3	5
ADD12	6	ADD13	6	ADD23	6	ADD24	6
3V3	7	ADD11	7	ADD21	7	ADD22	7
ADD10	8	ADD9	8	ADD19	8	ADD20	8
ADD8	9	TS	9	ADD17	9	ADD18	9
3V3	10	NET00231	10	NET00232	10	ADD16	10
3V3	11	RD_WR	11	NET00235	11	3V3	11
WE0	12	WE1	12	WE2	12	WE3	12
CSRAM	13	NET00241	13	NET00242	13	NET00274	13
NET00275	14	NET00276	14	NET00277	14	BOIP	14
NET00270	15	NET00271	15	NET00272	15	NET00273	15
NET00265	16	NET00267	16	NET00268	16	NET00269	16
NET00262	17	NET00263	17	NET00264	17	NET00265	17
NET00258	18	NET00259	18	NET00260	18	NET00261	18
NET00254	19	NET00255	19	NET00256	19	NET00257	19
NET00250	20	NET00251	20	NET00252	20	NET00253	20
5V	21	NET00247	21	NET00248	21	NET00249	21
VDD	22	5V	22	NET00245	22	NET00246	22

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DATA29	53	ADV	84	BDIP
DATA28	54	A0SP	85	TS
DATA27	55	OE	86	EO
DATA26	56	BME	87	RD
DATA25	57	GM	88	WR
DATA24	58	CE1	89	CLKOUT
DATA23	59	CE3	92	ADD12
DATA22	60	BMA	93	WE0
DATA21	61	BMA	94	WE1
DATA20	62	BMA	95	WE2
DATA19	63	BMD	96	WE3
DATA18	64	CE2	97	ADD11X
DATA17	65	CE1	98	CSRAM
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Notes:

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