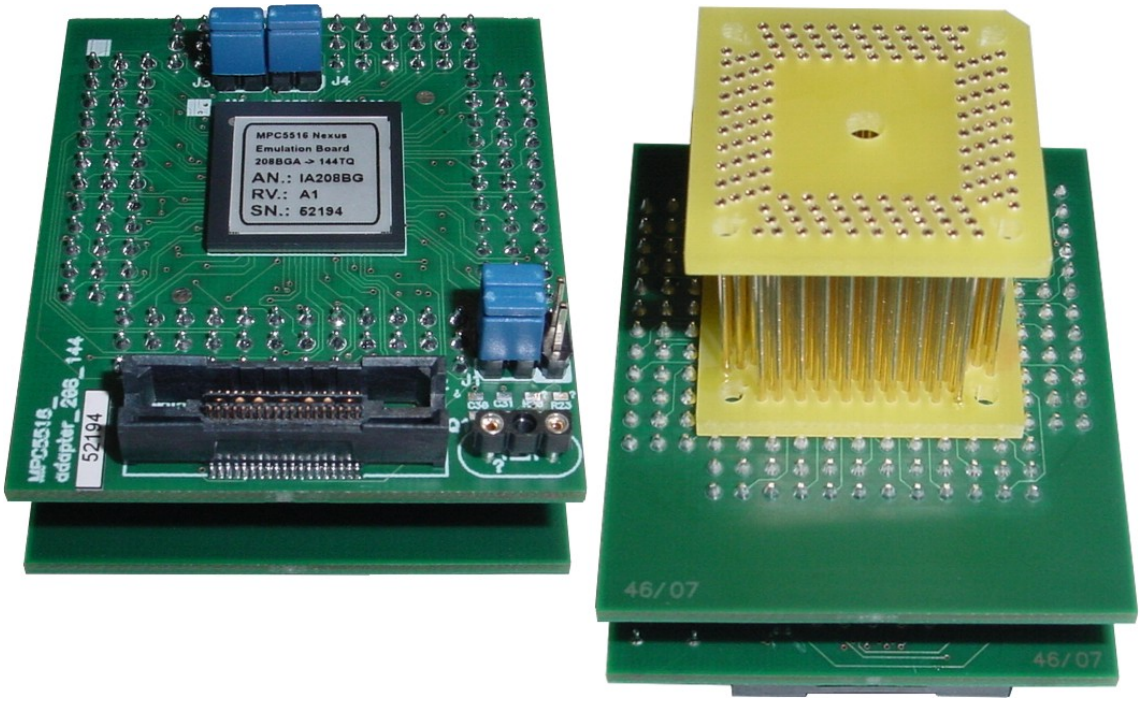
Nexus Emulation Board 208BGA – 144TQ

Ordering code	IA208BGA144TQ-5516



Target CPU package: T_QFP144

The original MPC5516 device has port F, on which alternate operations beside the default GPIO operation are possible. One of the possible operations is for it to be used as a Nexus port used for development. When a user connects an external development tool to the port F, this port is lost for the application.

This adapter is an alternative solution for the MPC5516 development. The Nexus Emulation Board is based on a MPC5516 device in the BGA208 package. The emulator connects to port F in the BGA208 device and then the port J from the BGA208 device is connected to port F, replacing the lost Port F signals of the MPC5516 device. Consequently, the target application must be adjusted in order to use the port J instead of port F to which the external development tool connects.

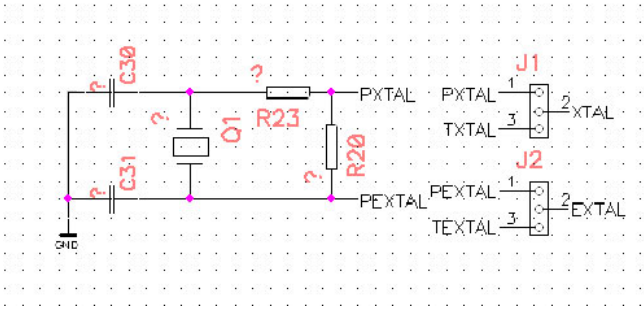
Original connection	Replacement connection
PF0 - PF15	PJ0 – PJ15

This solution can only be used as long as the replaced port F pins are used as GPIO in the target application. Also, interrupts on GPIO can not be used on port F.

Target Pad ID	Emulation Pad ID	Original SIU_PCR Address (port F)	Emulated SIU_PCR Address (port J)	Original SIU_GPDO Address (port F)	Emulated SIU_GPDO Address (port J)	Original SIU_GPDI Address (port F)	Emulated SIU_GPDI Address (port J)
PF0	PJ0	FFFE80E0	FFFE8140	FFFE8650	FFFE8680	FFFE8850	FFFE8880
PF1	PJ1	FFFE80E2	FFFE8142	FFFE8651	FFFE8681	FFFE8851	FFFE8881
PF2	PJ2	FFFE80E4	FFFE8144	FFFE8652	FFFE8682	FFFE8852	FFFE8882
PF3	PJ3	FFFE80E6	FFFE8146	FFFE8653	FFFE8683	FFFE8853	FFFE8883
PF4	PJ4	FFFE80E8	FFFE8148	FFFE8654	FFFE8684	FFFE8854	FFFE8884
PF5	PJ5	FFFE80EA	FFFE814A	FFFE8655	FFFE8685	FFFE8855	FFFE8885
PF6	PJ6	FFFE80EC	FFFE814C	FFFE8656	FFFE8686	FFFE8856	FFFE8886
PF7	PJ7	FFFE80EE	FFFE814E	FFFE8657	FFFE8687	FFFE8857	FFFE8887
PF8	PJ8	FFFE80F0	FFFE8150	FFFE8658	FFFE8688	FFFE8858	FFFE8888
PF9	PJ9	FFFE80F2	FFFE8152	FFFE8659	FFFE8689	FFFE8859	FFFE8889
PF10	PJ10	FFFE80F4	FFFE8154	FFFE865A	FFFE868A	FFFE885A	FFFE888A
PF11	PJ11	FFFE80F6	FFFE8156	FFFE865B	FFFE868B	FFFE885B	FFFE888B
PF12	PJ12	FFFE80F8	FFFE8158	FFFE865C	FFFE868C	FFFE885C	FFFE888C
PF13	PJ13	FFFE80FA	FFFE815A	FFFE865D	FFFE868D	FFFE885D	FFFE888D
PF14	PJ14	FFFE80FC	FFFE815C	FFFE865E	FFFE868E	FFFE885E	FFFE888E
PF15	PJ15	FFFE80FE	FFFE815E	FFFE865F	FFFE868F	FFFE885F	FFFE888F

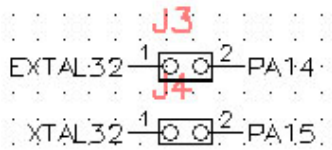
Jumper configuration

J1 and J2: clock source configuration



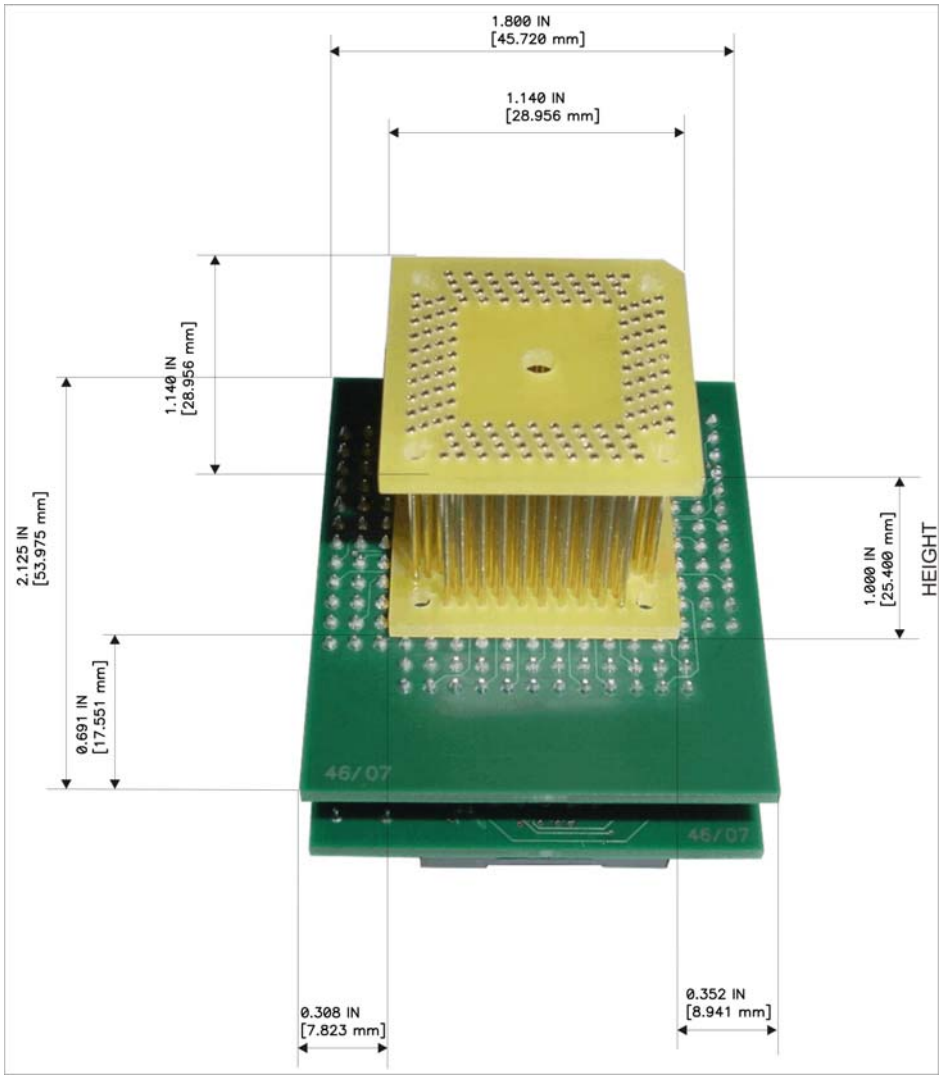
Jumpers J1 and J2 are used for clock source setting. When both jumpers are set to the position 1-2, the clock built on the Adapter is used and in this case, Q1, C30, C31, R20 and R23 must be populated. If the jumpers are set to 2-3, the clock from the target is used.

J2 and J3: 32 kHz clock selection



On the 144 pin package the EXTAL32 and XTAL32 pins are alternate function pins on PORTA14 and PORTA15 while on the 208 pin package these pins are alternate pins on PORTK0 and PORTK1. If the 32 kHz clock is required, jumpers J3 and J4 must be inserted.

Dimensions


1.800 IN
[45.720 mm]
1.140 IN
[28.956 mm]
1.140 IN
[28.956 mm]
2.125 IN
[53.975 mm]
0.691 IN
[17.551 mm]
1.000 IN
[25.400 mm]
HEIGHT
0.308 IN
[7.823 mm]
0.352 IN
[8.941 mm]
46/07
46/07

Schematic