Freescale M-Core Family On-Chip Emulation

This document is intended to be used together with the CPU reference manual provided by the silicon vendor. This document assumes knowledge of the CPU functionality and the terminology and concepts defined and explained in the CPU reference manual. Basic knowledge of winIDEA is also necessary. This document deals with specifics and advanced details and it is not meant as a basic or introductory text.

Contents

1 Introduction

The on-chip emulation (OnCE) port in Freescale's M·CORE M200 core is a JTAG-like (Joint Test Action Group) serial interface. A debugger communicates with and controls the M·CORE M200xx core through the cores OnCE port. In addition to other tasks, the debugger can cause the core to stop executing at a predefined instruction or data fetch or even to program a non-volatile memory device that might be connected to the core.

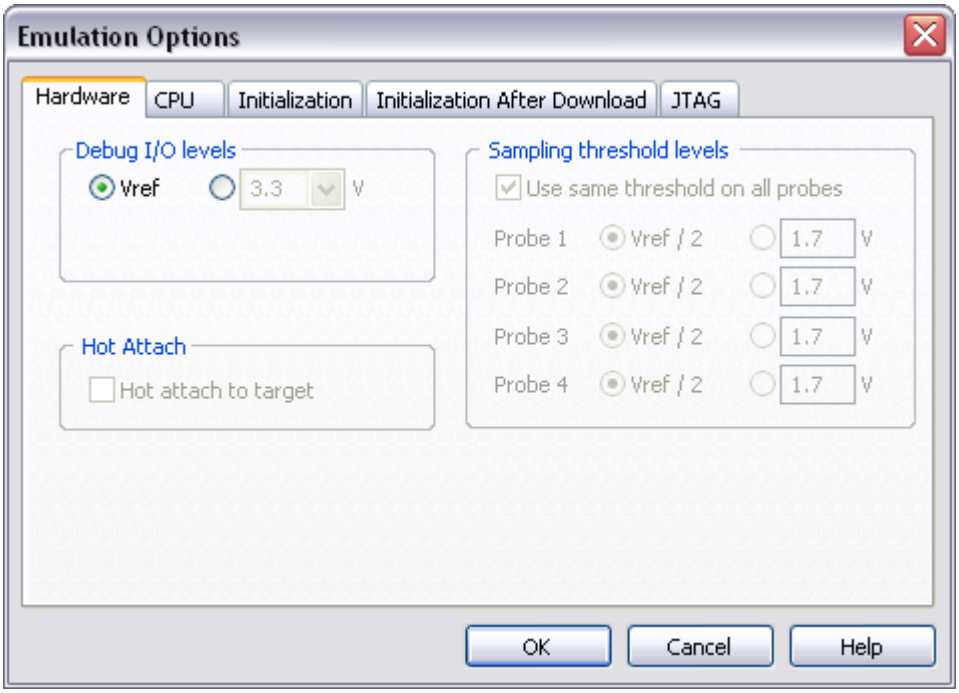
The OnCE debug module's serial interface expects a debug clock, TCK, that is no more than half of the frequency of the MMC20xx's CPU (central processor unit) clock, CLK.

Features

- 2 hardware breakpoints
- Unlimited software breakpoints
- Fast flash programming
- No real-time access

2 Emulation Options

2.1 Hardware Options



Emulation Options, Hardware page

Debug I/O levels

The development system can be configured in a way that debug (BDM/JTAG) signals are driven at 3.3V, 5V or target voltage levels. When 'Target Vcc' Debug I/O level is selected, a voltage applied to the belonging reference voltage pin (target debug connector) is used as a reference voltage for driving debug (BDM/JTAG) signals. Make sure that the target reference voltage pin is connected when 'Target Vcc' Debug I/O level is selected.

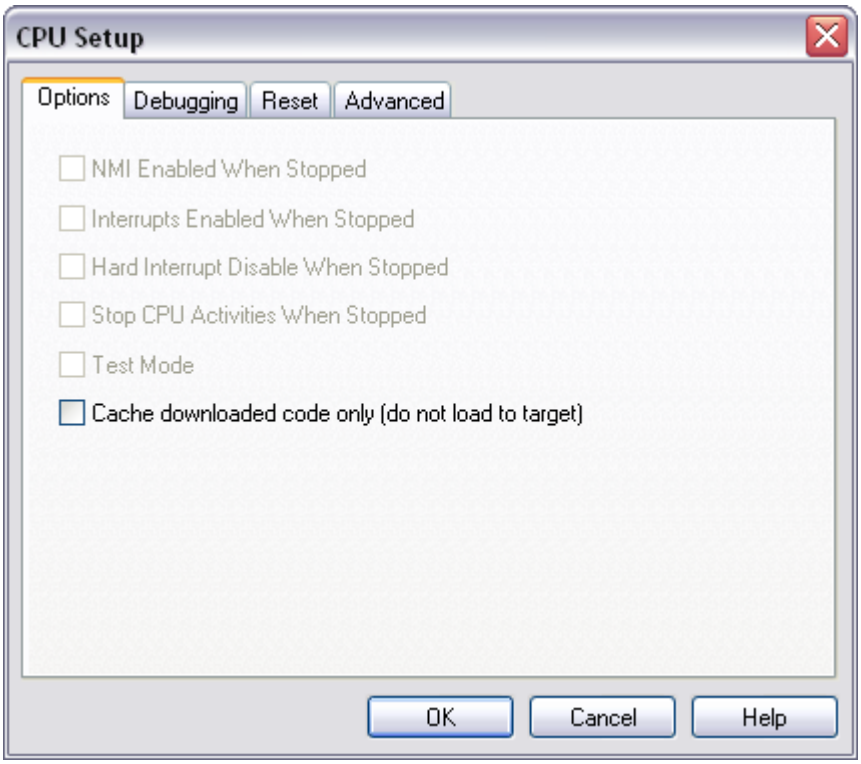
2.2 Initialization Sequence

Before the flash programming or download can take place, the user must ensure that the memory is accessible. This is very important since there are many applications using memory resources (e.g. external RAM, external flash), which are not accessible after the CPU reset. In that case, the debugger must execute after the CPU reset a so called initialization sequence, which configures necessary CPU chip selects and then the download or flash programming can actually take place. The user must set up the initialization sequence based on his application. Detailed information may be found in the Initialization Sequence help topic.

3 CPU Setup

3.1 General Options

The CPU Setup, Options page provides some emulation settings, common to most CPU families and all emulation modes. Settings that are not valid for currently selected CPU or emulation mode are disabled. If none of these settings is valid, this page is not shown.



General Options

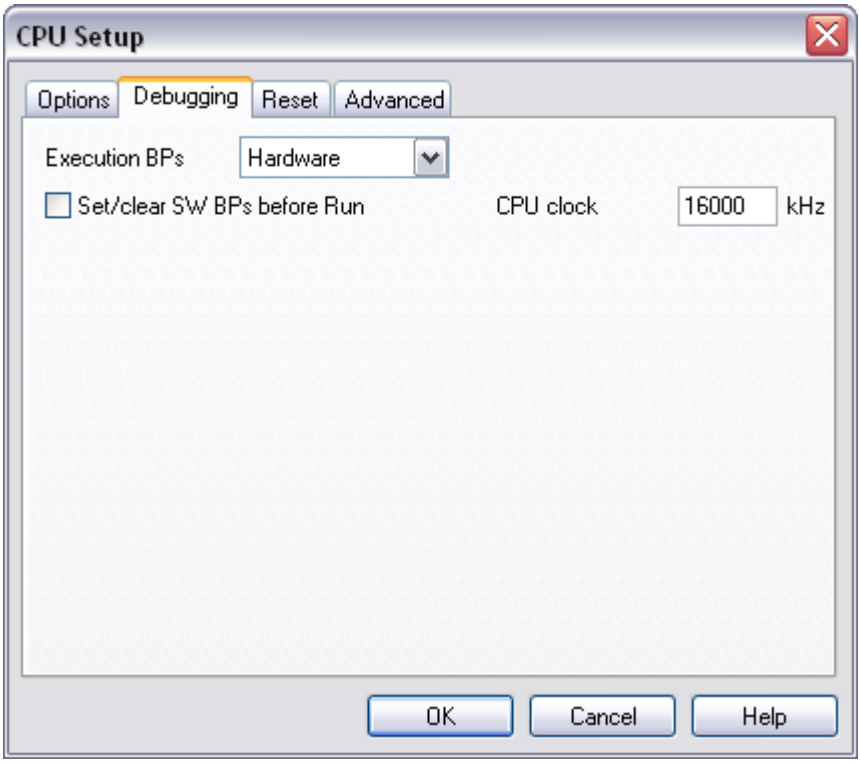
Cache downloaded code only (do not load to target)

When this option is checked, the download files will not propagate to the target using standard debug download but the Target download files will.

In cases, where the application is previously programmed in the target or it's programmed through the flash programming dialog, the user may uncheck 'Load code' in the 'Properties' dialog when specifying the debug download file(s). By doing so, the debugger loads only the necessary debug information for high level debugging while it doesn't load any code. However, debug functionalities like ETM and Nexus trace will not work then since an exact code image of the executed code is required as a prerequisite for the correct trace program flow reconstruction. This applies also for the call stack on some CPU platforms. In such applications, 'Load code' option should remain checked and 'Cache downloaded code only

(do not load to target)' option checked instead. This will yield in debug information and code image loaded to the debugger but no memory writes will propagate to the target, which otherwise normally load the code to the target.

3.2 Debugging Options



M-CORE Family Debugging Options

Execution Breakpoints

Hardware Breakpoints

Hardware breakpoints are breakpoints that are already provided by the CPU. The number of hardware breakpoints is limited to two. The advantage is that they function anywhere in the CPU space, which is not the case for software breakpoints, which normally cannot be used in the FLASH memory, non-writeable memory (ROM) or self-modifying code. If the option 'Use hardware breakpoints' is selected, only hardware breakpoints are used for execution breakpoints.

Note that the debugger, when executing source step debug command, uses one breakpoint. Hence, when all available hardware breakpoints are used as execution breakpoints, the debugger may fail to execute debug step. The debugger offers 'Reserve one breakpoint for high-level debugging' option in the Debug/Debug Options/Debugging' tab to circumvent this. By default this option is checked and the user can uncheck it anytime.

Software Breakpoints

Available hardware breakpoints often prove to be insufficient. Then the debugger can use unlimited software breakpoints to work around this limitation.

When a software breakpoint is being used, the program first attempts to modify the source code by placing a break instruction into the code. If setting software breakpoint fails, a hardware breakpoint is used instead.

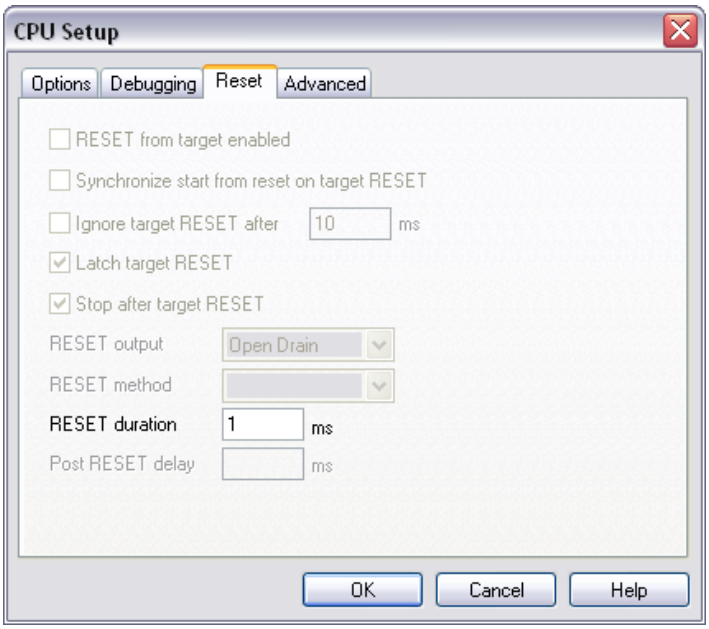
Set/clear SW BPs before Run

When the option is checked, then a software breakpoint is not set/cleared immediately, but is just remembered. Only when the CPU is set to running are the breakpoints committed. This way several breakpoints can be changed but only one re-FLASH operation takes place. This is especially noticeable in testIDEA operation with many stubs and also during a regular debugging session when several breakpoints are set/cleared within the same flash erase block.

CPU Clock

The CPU clock must be set here. A special divider is present on the CPU to ensure the correct programming frequency for the FLASH module, which is generated from the CPU clock. Since the CPU clock cannot be automatically detected, it must be set in this dialog. Note that this setting affects internal FLASH programming only.

3.3 Reset Options

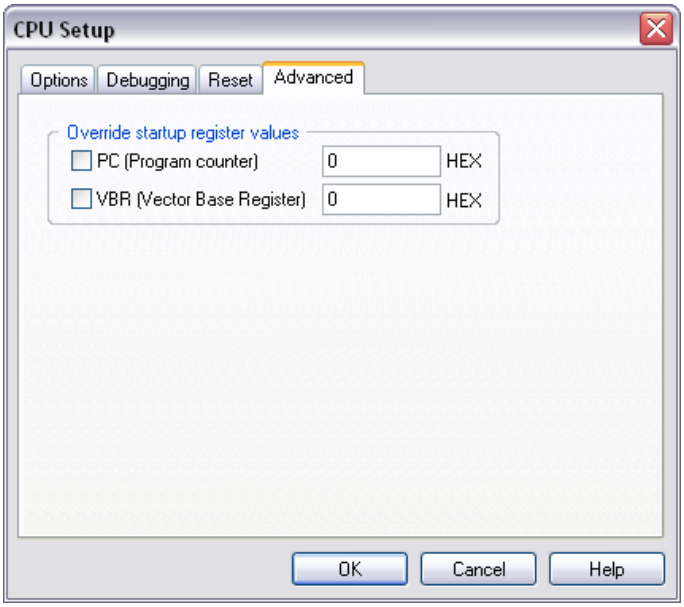


M-CORE Family Reset Options

RESET duration

Certain CPU supervisory circuits monitor the CPU reset line and detect if an external source pulled the line low. When the external source, in our case the software, releases the line, the supervisor circuit will continue to hold the line low for a predetermined time, depending on the circuit used. This reset active time should be entered in the 'Reset duration' entry. Otherwise, the CPU may appear dead to winIDEA, when actually it is still in reset.

3.4 Advanced Options



M-CORE Family Advanced Options

Override Startup Register Values

This option overrides the default Program Counter and Vector Base Register reset values with the values set.

4 Getting Started

Before powering on check the Power supply setting in Emulation Options/Hardware. Default is 3.3V, note however that certain newer devices operate at lower voltages and may no longer be 3.3V-tolerant. Use ‘Target’ setting in such case.

Disable watchdog with initialization sequence. Usually the watchdog timer will timeout after just a few seconds after reset is released, leaving very little time for user intervention. At the same time, don’t forget to disable or adequately service the watchdog timer in your software.

To enable code download user should provide some minimum memory access configuration. This can be trivial by merely setting the appropriate chip-select registers for flash or SRAM, or complicated and lengthy for DRAM. Note that there is no need for that if the target CPU has some internal RAM suitable for small test code.

It is recommended that CPU clock PLL is not modified in the initialization sequence as this may cause CPU debug port to fail. Instead, user code should do this in any case.

5 Known Issues

- The MMC2107 is not supported on the iC2000 BasePro Emulator.

6 Troubleshooting

When performing any kind of checksum, remove all software breakpoints since they may impact the checksum result.

Make sure that the power supply is applied to the target JTAG connector when ‘Target VCC’ is selected for Debug I/O levels in the Hardware/Emulator Options/Hardware tab, otherwise emulation fails or may behave unpredictably.